Heavy ion SEE test of 2 Gbit DDR3 SDRAM

Martin Herrmann, Kai Grürmann, Fritz Gliem, Heikki Kettunen, and Véronique Ferlet-Cavrois

Abstract—New generation 2 Gbit DDR3 SDRAMs from Micron, Samsung and Nanya have been tested under heavy ions. SEFIs significantly outweigh random SEU errors even at low LET; however, SEFIs can be mitigated by frequent reinitialization.

Index Terms—DDR3, Heavy ions, SDRAM, SEE

I. INTRODUCTION

For space borne memory applications, synchronous dynamic random access memories (SDRAMs) [4] [5] [6] are frequently used because of their high data rate compared to NAND flash memories. The third generation of double-data-rate SDRAMs, DDR3 SDRAM [2] [3], is available as commercial products by several memory manufacturers. DDR3 offers, in particular, the potential of higher densities, at present 4 Gbit compared to 2 Gbit for DDR2.

In the last years, heavy ion and proton single event test results [1] have been reported for DDR2 SDRAM [7] [8] [9] [10]. [10] also reports preliminary results on DDR3, but limited to 30 MeV protons.

In May 2011, we performed a test campaign at RADEF [11] with our newly developed DDR3 test bed. The primary purpose of the campaign was both to verify the proper functionality of the test bed and to characterize the DDR3 SDRAM behavior under heavy ions. The SEU and SEFI results for DDR3 devices of three manufacturers are summarized in this paper. These are the first heavy ion test results ever reported on DDR3 SDRAM.

II. MEMORY DEVICES

We tested memory devices from three different manufacturers:

1) Micron MT41J256M8 (2 samples, date code 0949)
2) Samsung K4B2G0846D (3 samples, date code 1006)
3) Nanya NT5CB256M8BN (3 samples, date code 1026)

This research has been supported by the European Space Agency, ESA-ESTEC, under contracts No 4200021711/08/NL/PA and 4000101358/10/NL/AF, and by the German Space Agency, DLR, under contract No FKZ 50 FM0707.

Martin Herrmann is with IDA, Institute of Computer and Network Engineering, Technische Universität Braunschweig, P. O. Box 3329, D-38106 Braunschweig, Germany (phone: +49 531 391 9679, e-Mail: mherrmann@ida.ing.tu-bs.de).
Kai Grürmann and Fritz Gliem are with IDA, Institute of Computer and Network Engineering, Technische Universität Braunschweig, P. O. Box 3329, D-38106 Braunschweig, Germany.
Heikki Kettunen is with the University of Jyväskylä, Department of Physics, Savonlinna 9, Jyväskylä, Finland.
Véronique Ferlet-Cavrois is with the European Space Agency, ESA-ESTEC, Keplerlaan 1, 2200AG Noordwijk, Netherlands.
matched to the die curvature measured after etching. The grinding process takes about eight hours per device.

For the whole process of opening and thinning, we achieved a yield of 75%.

### III. TEST FACILITY

The tests were conducted at the Radiation Effects Facility (RADEF) [11] in the Accelerator Laboratory at the University of Jyväskylä, Finland (JYFL). The facility provides a heavy ion beam line with a vacuum chamber for irradiation of electronic components. The ion cocktail available at RADEF is described in table I.

### IV. TEST EQUIPMENT

The head station of the RTMC6 testbed for DDR3 SDRAM, shown in fig. 1, is capable of operating a DUT in x4 or x8 configuration at a clock frequency of up to 400 MHz. It is based on a Xilinx ML605 [12] evaluation board, containing a Xilinx Virtex6 FPGA.

The ML605 is equipped with a small outline dual inline memory module (SODIMM) socket designed for commercially available memory modules. Since thinned devices cannot be soldered, we developed a DUT adapter which connects to the SODIMM slot and contains a zero insertion force (ZIF) FBGA socket suitable for DDR3 SDRAM devices. The DUT adapter also contains circuitry for switching power to the DUT.

The SDRAM is controlled by Xilinx’ DDR3 memory controller (MIG) software [13].

The FPGA contains a custom design which writes a (i) constant, (ii) counting or (iii) pseudo-random pattern to the memory, reads the data from the memory and compares it to the original pattern. If the data is different from the pattern, an error vector is generated and transmitted to a PC via a high speed USB connection.

Since the memory device has a higher data transfer rate than the USB connection, error vectors have to be buffered in a FIFO in order to be able to handle large runs of consecutive errors without slowing down the test.

On the PC, an error map (fig. 2) is displayed for preliminary visual analysis, along with a total error count and various statistics. For later analysis, the data is stored on a hard disk.

The FPGA and the power regulators dissipate several watts of heat. For tests in vacuum, we devised a water cooler consisting of copper block placed above the board. The block is equipped with several threaded bolts to match the different heights of the components to be cooled. The water circulation is taken out of the vacuum chamber through a flange.

### V. TEST DESCRIPTION

The tests were performed with the head station in vacuum in DLL on mode at a clock frequency of 333.3 MHz.

A 7.8 µs auto-refresh interval was used, as specified by the JEDEC standard [3]. The whole memory device was tested using a pseudo-random pattern.

Before each test run, the pattern is written to the memory and verified to detect “stuck bits”. Stuck bits are cells which always read as a fixed value, regardless of the data written to the cell.

After that, one of three tests is performed:

- **Storage mode (M3):** the device is irradiated without any activity (except required idle activity like refresh). After irradiation, the data is read.
- **Read mode (M1):** the device is irradiated while continuously reading the data. Errors introduced by irradiation accumulate.
- **Marching mode (M2):** the device is irradiated while data is continuously written and read. Contrary to M1 mode, errors introduced by irradiation do not accumulate since the data is overwritten in each loop.

In earlier test campaigns with DDR2 SDRAM, periodic reinitialization of the memory device has been found to significantly reduce the number of SEFIs [9]. Fig. 3 shows the effect of reinitialization on the SEFI cross section for a Micron DDR2 device in read mode with Argon. A short initialization was inserted after a given number of memory rows (1024 words) had been read. Reinitialization reduced the cross section by almost two orders of magnitude if performed at least every 128 rows; more frequent reinitialization did not lead to any improvement.

Since Xilinx’ DDR3 controller does not support reinitialization during operation, this could not be performed for DDR3 SDRAM in this campaign. However, it is possible to reset the SDRAM controller, which causes a startup initialization. While the JEDEC standard does not guarantee that the data is retained over a reset, we found that in practice, no data is lost until the reset condition is held for several seconds, provided that the device is kept powered.

---

**TABLE I**

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy (MeV)</th>
<th>Range in Si (µm)</th>
<th>LET (surface) (MeV cm²/µg)</th>
<th>LET (70 µm Si) (MeV cm²/µg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>¹⁵Ν⁺⁴</td>
<td>139</td>
<td>202</td>
<td>1.8</td>
<td>2.0</td>
</tr>
<tr>
<td>²⁰Ne⁺⁶</td>
<td>186</td>
<td>146</td>
<td>3.6</td>
<td>4.8</td>
</tr>
<tr>
<td>³⁰Si⁺⁸</td>
<td>278</td>
<td>130</td>
<td>6.4</td>
<td>8.2</td>
</tr>
<tr>
<td>⁴⁰Ar⁺¹²</td>
<td>372</td>
<td>118</td>
<td>10.1</td>
<td>14.3</td>
</tr>
<tr>
<td>⁵⁶Fe⁺¹⁵</td>
<td>523</td>
<td>97</td>
<td>18.5</td>
<td>27.3</td>
</tr>
<tr>
<td>⁸²Kr⁺²²</td>
<td>768</td>
<td>94</td>
<td>32.1</td>
<td>40.5</td>
</tr>
<tr>
<td>¹³¹Xe⁺³⁵</td>
<td>1217</td>
<td>89</td>
<td>60.0</td>
<td>61.5</td>
</tr>
</tbody>
</table>

---

Fig. 2. The error map shown for visual inspection during the test. SEUs, row SEFIs and column SEFIs can be recognized, but the precise number of errors of each class can not be determined, because each pixel summarizes a total of 16384 bits.
To examine the effect of reinitialization, the SDRAM device was reset and read a second time after each test run. During initialization, the memory controller overwrites the first 16 words of the first row in the first bank for calibration of the data line timing. These locations were ignored during analysis.

First, all eight samples were tested with Argon and Neon. After verifying that the behavior of different samples of the same manufacturer is sufficiently similar, subsequent tests were performed with a reduced number of samples.

VI. TEST RESULTS

A total of 642 runs were recorded. Each of these runs was analyzed with respect to the following error types (fig. 4):

- **Class A errors**, or **SEUs**, are isolated errors, typically caused by a hit in the memory array. They usually affect only one single bit in a word, although heavier ions like Krypton and Xenon can lead to two or three bit errors in a single word. These multi-bit errors are counted as a single class A error.
- **Class B errors**, either **row** or **column SEFIs**, are many bit errors in a single row or column, typically caused by a hit in the control circuits. Any row or column exhibiting this pattern is counted as a single class B error.
- **Class C errors**, or **device SEFIs**, are a persistent loss of functionality, also caused by a hit in the control circuits. Device SEFIs can only be resolved by a power cycle or a reinitialization.
- **Class D errors** are destructive failures, permanently damaging the device.

Additionally, devices may exhibit single event latch-up (SEL) behavior under irradiation. Neither destructive failures nor latch-ups were observed for any of the tested devices in any test mode.

A. Cross sections

Fig. 5 shows the cross sections for SEUs, row SEFIs and column SEFIs in storage mode (M3). A open symbol indicates a run without any errors of the respective kind.

For all error species, Samsung devices showed substantially less errors than Micron and Nanya devices. The cross sections for column errors in marching mode (M2), shown in fig. 6, are similar to the ones in storage mode (fig. 5(c)). The same similarity was found for all error classes.

The important message is that the number of row and column SEFIs is in the same order of magnitude as the number of SEUs. As each SEFI causes several (typically hundreds) of bit errors, the errors induced by SEFIs outweigh the number of random errors by far, even at low LET.

Fig. 7 shows the SEU cross sections of the DDR3 devices we tested, compared to the cross sections of DDR2 devices tested in earlier campaigns. Of all devices, Samsung DDR3 devices showed the most favorable cross section. The SEU cross section of Micron DDR3 devices is reduced, compared
to Micron DDR2 devices, but still substantially larger than that of Samsung DDR3 devices.

Fig. 6. Cross sections for column SEFIs in marching mode (M2)

Fig. 7. SEU cross section of DDR2 and DDR3 devices compared

B. Effects of reinitialization

After each test, the device was read, reset to cause a reinitialization, and read again. Fig. 8 shows the cross sections for bit errors (not distinguishing between the different error classes) before and after reinitialization.

Two contrary results have been found:

- For Micron and Nanya parts, the number of errors decreased substantially by a factor of about 200 to 2000 after reinitialization.
- For Samsung parts, the number of errors was either unchanged or increased slightly (by a factor of about 1 to 2) after reinitialization. This corresponds to the fact that Samsung devices showed nearly no SEFIs (fig. 5).

VII. Future work

DDR3 SDRAM supports various power modes (e.g. active power down, precharge power down [3]) which we want to further cover in future tests.

Reinitialization has been shown to substantially reduce the number of errors for Micron and Nanya devices, but not for Samsung devices. Therefore, we intend to insert, in our test sequences, an abbreviated initialization at regular intervals (storage mode) or during read and write operation (read and marching modes), as for DDR2.

Since Xilinx’ DDR3 controller supports neither reinitialization nor different power modes, we plan to develop a specialized DDR3 SDRAM controller for testing purposes.

Another objective for future campaigns is to also test devices from Hynix and Elpida, which could not be procured for this campaign.

VIII. Conclusion

We tested DDR3 SDRAM at 333.3 MHz in DLL on mode. The main results are:

- The frequency of SEFIs is similar to the frequency of SEUs.
- The number of random errors (SEUs) is outweighed by the number of errors caused by SEFIs.
- Samsung devices showed considerably fewer SEUs and SEFIs than Micron and Nanya devices.
- For Micron and Nanya devices, reinitialization is an effective means for reducing the number of SEFI related errors, as with DDR2 SDRAM.
- No destructive failures or latch-ups occurred.

REFERENCES