Heavy Ion sensitivity of 16/32-Gbit NAND-Flash and 4-Gbit DDR3 SDRAM

Kai Grüermann, Martin Herrmann, Fritz Gliem, Hagen Schmidt, Gilbert Leibeling, Heikki Kettunen, and Véronique Ferlet-Cavrois

Abstract—16/32-Gbit NAND-Flash and 4-Gbit DDR3 SDRAM memories have been tested under heavy ion irradiation. At high LET, 25 nm NAND-Flash show MBUs at normal incidence. Techniques for SEFI mitigation in DDR3 SDRAM are studied.

Index Terms—NAND-Flash, DDR3-SDRAM, SEE, MBU.

I. INTRODUCTION

Two storage technologies, commercial SDRAM [1] and commercial NAND-Flash [2], are in use for the implementation of space mass memories. The device capacity is rapidly growing due to continuous shrinking of the feature size. 4-Gbit DDR3 SDRAM and 32-Gbit SLC NAND-Flash represent the current generation. Typically, devices of the most recent generations only are on the market. The devices of older generations, for example 8-Gbit SLC NAND-Flash, are becoming obsolete. This fact forces the designers of space mass memories to base the design of future systems on the most recent device generation, even if their better performance in density and speed is not exploited. Instead, in many cases, the new designs have to live with unfavorable characteristics of the new devices, such as increased sensitivity to radiation induced Single Event Effects (SEE) [3].

The constraints to follow the progress in technology from generation to generation imply that radiation assessment of the new generation devices has to be performed and taken into account for the design of future mass memory systems.

For that purpose, in January 2012, we performed a heavy ion SEE test of two types of 16-Gbit and 32-Gbit SLC NAND-Flash and two types of 4-Gbit DDR3 SDRAM memories (see Table I) at the RADEF facility in Jyväskylä, Finland. The results are compared to SEE data obtained on previous memory generations, i. e. 8-Gbit NAND-Flash and 2-Gbit DDR3 (see Table II).

II. DUT PREPARATION

DDR3 silicon dies are encapsulated flipchiped in plastic ball grid packages. The active die zone is situated to the pads in order to reduce the lead inductance (Fig. 1). Before irradiation, and because of the limited range of the used heavy ions, the plastic has to be removed down to the back surface of the die, and the die has to be thinned from initially about 300 µm to about 60 µm. Two different methods, A and B, have been used for the preparation of the Devices Under Test (DUT).

With method A, the plastic above the back surface of the
die and a large part of the plastic rim around the edges of the die are removed by wet chemical etching. Thereafter the die is found to be not exactly flat but warped. The surface height varies by up to 40 µm. The height contour is measured, and the rotating blade tool used for grinding follows the measured contour. Details of method A are described in [4].

In contrast, method B enforces the die in an exactly flat position. This supports grinding and polishing without the need for contour following of the abrasive tool. At first, the layer thickness of the plastic encapsulation and the silicon die to be grinded is determined, based on the cross section of a sample chip (Fig. 2). The devices are bilaterally putted between glass plates. Planarity and parallelism of the chip surface during the mechanical processing is guaranteed by fixing the devices between the glass plates. The deployed machine used (DISCO DAG 810) enables a thickness tolerance of ±5 µm.

In the first grinding work step, plastic layer and glass plate were grinded down to the silicon surface of the DDR3 chip. After reaching the silicon surface, the target thickness of the silicon die is entered to the machine and, after that, the silicon die as well as the plastic encapsulation are thinned. Inevitably, the grain size of the tool must be carefully adapted for the silicon material. If the grain size is too rough, microscratches due to the high mechanical stress lead to imperfections in the functionality up to the destruction of the DDR3 chip.

Mechanical stress by the one side opening of the plastic encapsulation leads after the detaching of the element from the glass plate, to a bowed chip surface as described in method A. But this bowing arising after the mechanical processing does not influence the functionality of the memory.

In both methods the yield fluctuates between 30% and 70%. The main advantage of method B is that 10 samples can be thinned in one batch.

Method B has been used for most of the DUTs of our last RADEF campaign.

The NAND-Flash DUTs have been opened by drop etching with fuming nitric acid.

III. ERROR CLASSIFICATION AND CORRECTION

Fig. 3 shows the classification scheme for Single Event Errors.

Class A comprises all random SEUs over the address space distributed as single-bit errors up to small error clusters such as multi-bit or multi-symbol errors.

Symbol is a data item associated with the data width of a single memory device, in many cases one byte.

Space memories are equipped with a symbol oriented error correction. The word comprises \( n \) symbols, divided into \( k \) (e. g. 8) data symbols and \( n - k \) (e. g. 2) parity symbols, distributed over the \( n \) devices of the respective word group (WG).

A word group comprises all words of the same set of \( n \) devices, in case of 512Mx8 DDR3-SDRAM 512M words.

Any error that only affects one symbol of the word is correctable. The corruption of two symbols is 100 % detectable. The probability of the coincidence of 2 SEUs in the same word is extremely low. The presence of SEUs in a word group typically delivers an only minor impairment of the word group performance by non-correctable multi-symbol errors.

For example, the relatively moderate increase of the random SEU cross section, observed in 4-Gbit DDR3 and 16-/32-Gbit NAND-Flash (see Sections V and VII) compared to the previous 2-Gbit DDR3 and 8-Gbit NAND-Flash generation, is not of much concern.

In class B, transient SEFIs are categorized. Transient SEFIs appear as row errors, column errors, or, in case of NAND-Flash, block errors. Class B SEFIs originate from the internal device control and interface circuitry. They disappear with the next access.

A row or a column error in the respective word group significantly increases the probability for words affected by two or more symbol errors. Class B SEFIs can be made ineffective by error correction and access repetition.

In class C, Persistent SEFIs are categorized. The SEFI error pattern is removable only by an intervention of the memory controller or, as a last resort, by power cycling. This implies data loss for SDRAM in contrast to NAND-Flash. Less stringent interventions are re-initialization, and, for DDR3, DLY reset, ZQ calibration [5], device reset and memory controller reset. For the latter two actions, data retention is not guaranteed by the DDR3 standard [6].

Class C SEFIs can be differentiated according to the error pattern, such as row, column, device, and/or according to the
chances of SEFI removal without data loss.

Class C device SEFIs provide the highest potential to generate non-correctable words by coincidence of the erroneous symbols of the SEFI device with random SEUs in other devices of the word group. Therefore, attempts to remove the SEFI without data loss should be started soon after SEFI detection, namely before random SEUs accumulate in the other devices of the word group.

For SDRAM, the worst case is when power cycling is necessary to remove the SEFI, which corrupts the data stored in the affected device. In contrast, it is an important advantage of NAND-Flash that SEFI removal by power cycling does not disturb the stored data.

Accordingly, one goal of our test was to study for DDR3 SDRAM, the feasibility of Class C SEFI removal without data loss.

IV. TEST FACILITY AND TEST EQUIPMENT

Table III presents the characteristic data of the RADEF ion cocktail.

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy [MeV]</th>
<th>LET, Surface [MeV cm²/mg]</th>
<th>LET, 50 μm [MeV cm²/mg]</th>
<th>Range [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>¹⁵N⁺⁴⁺</td>
<td>139</td>
<td>1.8</td>
<td>2.1</td>
<td>202</td>
</tr>
<tr>
<td>²⁰Ne⁺⁶⁺</td>
<td>186</td>
<td>3.6</td>
<td>4.4</td>
<td>146</td>
</tr>
<tr>
<td>³⁰Si⁺⁶⁺</td>
<td>278</td>
<td>6.4</td>
<td>7.8</td>
<td>130</td>
</tr>
<tr>
<td>⁴⁰Ar⁺¹²⁺</td>
<td>372</td>
<td>10.1</td>
<td>12.6</td>
<td>118</td>
</tr>
<tr>
<td>⁵⁰Fe⁺¹⁵⁺</td>
<td>523</td>
<td>18.5</td>
<td>24.3</td>
<td>97</td>
</tr>
<tr>
<td>⁸²Kr⁺²²⁺</td>
<td>768</td>
<td>32.1</td>
<td>39.2</td>
<td>94</td>
</tr>
<tr>
<td>¹³¹Xe⁺³⁵⁺</td>
<td>1217</td>
<td>60.0</td>
<td>69.2</td>
<td>89</td>
</tr>
</tbody>
</table>

The basic structure of the NAND-Flash test bed is described in [8].

The DDR3 test bed is largely the same as used in our last test campaign [9]. Instead of the Xilinx DDR3 controller, however, the current version of our test equipment employs a custom DDR3 controller developed at IDA. In contrast to the Xilinx controller, this new controller allows to perform an assortment of different operations (writing mode registers, resetting the DLL of the DDR3 device and performing a ZQ calibration) at arbitrary times and in arbitrary order.

V. CROSS SECTIONS OF 16-GBIT / 32-GBIT NAND-FLASH

A. Random SEU Cross Section

Fig. 4 shows the static random SEU cross section of the Micron 16-Gbit and 32-Gbit device with 25 nm feature size. For comparison, the values for the Micron 50 nm 8-Gbit device as well as for the Samsung 8-Gbit device[10] are also shown.

The static SEU cross sections of the 16-Gbit and the 32-Gbit NAND-Flash are nearly identical. At low LET, they exceed the SEU cross-section of the Micron 8-Gbit NAND-Flash by several orders of magnitude. In particular, the threshold LET is substantially lower than the lowest LET of the available RADEF ion cocktail (nitrogen, 1.8 MeV cm²/mg). At high LET, the difference between cross sections is reduced to less than one order of magnitude.

The area of the 16-Gbit chip is 0.9 cm², i.e., 5.24 · 10⁻¹¹ cm²/bit = (72 μm)²/bit. The measured random SEU cross section exceeds this value, even at low LET. This indicates that single hits induce multiple random SEUs. The inspection of the error records revealed that, in most cases, the same bit in the same byte of adjacent rows is corrupted. Multi-bit errors in the same byte are rare. Fig. 5 shows the increase of the share of adjacent row SEUs with LET.

Stuck bits are noted in increasing number at higher LET – about 20% of the random SEUs at Xenon.

B. SEFI Cross Section

In Fig. 4, one of the three Samsung 8-Gbit lots, lot E, shows nearly the same curve as the Micron 8-Gbit device. However, for unknown reasons, the lots F and G exhibit a substantially lower static cross section. We never observed such a significant difference between devices of the same type before.

Fig. 5. Share of adjacent row SEUs
At a later test in April, we observed DFs even at Iron and also at Krypton, as earlier for the 8-Gbit devices.

Fig. 6 shows, for the 16-Gbit device in Read Mode, the class B cross section of (i) column SEFIs, (ii) row SEFIs and (iii) block SEFIs. The respective cross sections of the 32-Gbit device are very similar.

![Fig. 6. Class B SEFI cross section in read mode, Micron 16-Gbit NAND-Flash](image)

In contrast to read mode, the marching mode combines erase, write and read cycles. Fig. 7 shows the class B SEFI cross section in marching mode, which is somewhat larger than in read mode due to the additional contribution of the erase and write related operations. In storage mode, SEFIs appear at the first readout, but they disappear at a second readout after power cycling.

![Fig. 7. Class B SEFI cross section in marching mode](image)

A portion of the static random SEUs disappears with time due to annealing. Fig. 8 shows the annealing over the first 80 days. SEUs induced at low LET anneal more significantly than SEUs induced at high LET, in agreement with our previous observations on 1-, 2- and 4-Gbit devices [11]. Nitrogen induced random SEUs show a very strong annealing.

Fig. 8. Annealing over time

![Fig. 8. Annealing over time](image)

VI. CROSS SECTIONS OF 4-GBIT DDR3 SDRAM

A. Random SEU Cross Section

Fig. 9 shows the random SEU cross section of the Elpida and the Samsung 4-Gbit DDR3 SDRAM, and for comparison of the Samsung 2-Gbit DDR3 device[9].

![Fig. 9. DDR3 static random SEU cross section](image)

B. SEFI Cross Section

The DDR3 SDRAM showed neither DF nor SEL. However, a large number of Persistent Device SEFIs (class C), and in particular of those with the largest damaging potential, namely Persistent Device SEFIs, were observed. For example, Fig. 10 shows the cross section of the 4-Gbit DDR3 from Elpida. Even low LET neon ions induce Persistent Device SEFIs.

![Fig. 10. DDR3 Persistent Device SEFI cross section](image)

VII. DDR2/3 SEFI REMOVAL

DDR2 SDRAM is prone to Persistent SEFIs [4]. In particular, device SEFIs is dangerous. In this case, every random
SEU in another device of that word group produces a non-correctable symbol error. Therefore, we checked how the Persistent SEFIs can be removed for several DDR2 and DDR3 devices at Krypton (Fig. 11). The bar for the Micron 2-Gbit DDR2 device displays that 50% (10 of the 20 Device SEFIs) could be removed by measures of subgroup C1, i.e., guaranteed without data loss. Four of the remaining 12 Device SEFIs (= 20% of 20) could be removed by measures of subgroup C2, where data retention is not guaranteed by the manufacturer, but in practice, no data loss took place. The remaining 6 Device SEFIs disappeared only after power cycling and with associated data loss. This last resort measure always worked.

Then we directed the focus on the device of our main interest at that time, namely the Elpida 4-Gbit DDR3 (Fig. 11 right). At all LET about 20% of the Device SEFIs are resolvable with guaranteed data retention (C1), and at low LET up to Argon all others with C2 actions, i.e., with data retention in practice, but without manufacturer’s guarantee. At Iron and Krypton, a small percentage of the Device SEFIs is removable by power cycling only.

![Graph showing device SEFIs removal](image)

Tables IV and V illustrate the random SEU rate before and after correction and also the SEFI event rates for the heavy ion spectrum of two typical orbits with a shielding of 1 g/cm² ≈ 3,705 nm aluminum. The rates were calculated with OMERE 3.5.1.3 [12].

For the DDR3, the surface area of the sensitive volume is derived from the saturation value \( \sigma_{\text{sat}} \) of the measured cross section curve (Fig. 9):

\[
a^2 = \sigma_{\text{sat}} = 4.4 \cdot 10^{-12} \text{ cm}^2/\text{bit} = (21 \text{ nm})^2/\text{bit}
\]

The traditional common practice assumption of the depth \( c = 1 \mu\text{m} \) delivers an unrealistic side to depth ratio of \( c/a \approx 50 \). Obviously, it is not applicable to high density memory devices. In [13], a default ratio of \( c/a = 0.1 \) is recommended.

We derived the depth \( c \) of the sensitive volume from (i) the number of electrons in a completely filled storage capacitor and from (ii) the LET_{50%} value of the measured cross section curve:

\[
\sigma(\text{LET}_{50%}) = \frac{1}{2} \cdot \sigma(\text{LET}_{\text{sat}})
\]

\[
\text{LET}_{50%} = 30 \text{ MeV cm}^2/\text{mg}
\]

On average, the critical charge \( Q_c \) of a storage cell is about one third of its total charge, namely about \( \frac{1}{3} \cdot 60000 \text{ electrons} = 20000 \text{ electrons} \).

The critical charge varies from cell to cell, and for a given cell from time to time, for numerous reasons such as (i) variation of the bit line capacity, (ii) cross talk between bit lines, (iii) fluctuation of the sense amplifier reference, (iv) statistical variation of the deposited charge in thin layers, etc.

The starting point of the cross section curve represents cells of \( Q_{c,\text{min}} \), the saturation point cells of \( Q_{c,\text{max}} \), and the 50% point cells of \( Q_{c,\text{average}} \).

The expression

\[
\frac{Q_{c,\text{av}}}{e} = \frac{\text{LET}_{50%} \cdot \frac{\rho_{\text{Si}} \cdot c}{3.62 \text{ eV}}}{\text{MeV cm}^2/\text{mg} \cdot \frac{c}{\text{nm}}} \cdot \frac{1}{1.56 \cdot 10^{-2}}
\]

can be rewritten as

\[
\frac{Q_{c,\text{av}}}{e} = \frac{\text{LET}_{50%}}{\text{MeV cm}^2/\text{mg}} \cdot \frac{c}{\text{nm}} \cdot 1\text{.56} \cdot 10^{-2}
\]

With LET_{50%} = 30 MeV cm²/mg and \( Q_{c,\text{av}}/e = 20000 \), we get

\[
c \approx 10 \text{ nm}; \quad \frac{c}{a} \approx 0.5
\]

A Reed Solomon Single Symbol Correction applied to a word group of \( n = 8 + 2 \) byte-wide devices is assumed. Because of the low LET threshold, an additional contribution by direct proton ionization can not be excluded.

<table>
<thead>
<tr>
<th>Table IV</th>
<th>Error Rates for 800 km/98° Polar Orbit</th>
</tr>
</thead>
<tbody>
<tr>
<td>GCR (ISO, quiet)</td>
<td>Solar Flare Worst Week</td>
</tr>
<tr>
<td>Micron 16-Gbit NAND-Flash</td>
<td></td>
</tr>
<tr>
<td>Random SEU [bit/day]</td>
<td>3.1 \cdot 10^{-10}</td>
</tr>
<tr>
<td>Word Error Rate(a) [word/day]</td>
<td>9.7 \cdot 10^{-16}</td>
</tr>
<tr>
<td>SEFI [dev/day]</td>
<td>1.8 \cdot 10^{-3}</td>
</tr>
<tr>
<td>Elpida 4-Gbit DDR3 SDRAM</td>
<td></td>
</tr>
<tr>
<td>Random SEU [bit/day]</td>
<td>3.1 \cdot 10^{-12}</td>
</tr>
<tr>
<td>Word Error Rate(a) [word/day]</td>
<td>2.8 \cdot 10^{-20}</td>
</tr>
<tr>
<td>Class C, Device(b) [dev/day]</td>
<td>1.4 \cdot 10^{-5}</td>
</tr>
<tr>
<td>Class C, Device(c) [dev/day]</td>
<td>7.0 \cdot 10^{-7}</td>
</tr>
<tr>
<td>Samsung 4-Gbit DDR3 SDRAM</td>
<td></td>
</tr>
<tr>
<td>Random SEU [bit/day]</td>
<td>4.2 \cdot 10^{-12}</td>
</tr>
<tr>
<td>Word Error Rate(a) [word/day]</td>
<td>5.1 \cdot 10^{-20}</td>
</tr>
<tr>
<td>Class C, Device(d) [dev/day]</td>
<td>1.3 \cdot 10^{-6}</td>
</tr>
</tbody>
</table>

\(a\) post correction
\(b\) without periodic reinitialization
\(c\) with periodic reinitialization
\(d\) no change by reinitialization

VIII. Discussion
Both random SEUs and SEFIs contribute to the overall rate of erroneous symbols.
In a NAND-Flash device, a block SEFI disturbs up to 64 pages (rows) of 4k bytes each, namely 256k bytes. A row SEFI affects up to 4k bytes and a column SEFI up to 64 bytes of the respective block. Power cycling at the transition from block to block limits the extension of column and device SEFIs to one block.

Accordingly, we calculate the SEFI generated SEU cross section by accumulating the column cross section times 4k and the block and device cross section by accumulating the column cross section times 64, respectively.

![Fig. 12. SEFI generated SEU Cross Section in Read Mode, Micron 16-Gbit NAND-Flash](image)

FIG. 12. SEFI GENERATED SEU CROSS SECTION IN READ MODE, MICRON 16-GBIT NAND-FLASH

<table>
<thead>
<tr>
<th>Tab. V</th>
<th>ERROR RATES FOR 1 AU ORBIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GCR (ISO, quiet)</td>
</tr>
<tr>
<td>Micron 16-Gbit NAND-Flash</td>
<td></td>
</tr>
<tr>
<td>Random SEU [bit/day]</td>
<td>1.7 \times 10^{-9}</td>
</tr>
<tr>
<td>Word Error Ratea [word/day]</td>
<td>8.3 \times 10^{-15}</td>
</tr>
<tr>
<td>SEFI [dev/day]</td>
<td>5.5 \times 10^{-3}</td>
</tr>
<tr>
<td>Elpida 4-Gbit DDR3 SDRAM</td>
<td></td>
</tr>
<tr>
<td>Random SEU [bit/day]</td>
<td>1.1 \times 10^{-11}</td>
</tr>
<tr>
<td>Word Error Ratea [word/day]</td>
<td>3.4 \times 10^{-19}</td>
</tr>
<tr>
<td>Class C, Deviceb [dev/day]</td>
<td>4.2 \times 10^{-5}</td>
</tr>
<tr>
<td>Class C, Deviced [dev/day]</td>
<td>2.2 \times 10^{-6}</td>
</tr>
<tr>
<td>Samsung 4-Gbit DDR3 SDRAM</td>
<td></td>
</tr>
<tr>
<td>Random SEU [bit/day]</td>
<td>1.6 \times 10^{-11}</td>
</tr>
<tr>
<td>Word Error Ratea [word/day]</td>
<td>7.0 \times 10^{-10}</td>
</tr>
<tr>
<td>Class C, Deviced [dev/day]</td>
<td>4.0 \times 10^{-6}</td>
</tr>
</tbody>
</table>

1E-8 1E-6 1E-4 1E-2 1E+0

\sigma_{SEFI} [cm^2 device^{-1}]

erroneous symbols per block

erroneous symbols per row

sefi generated SEU cross section

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LET particles like alphas and protons, will have an only short lifetime and therefore will be less dangerous than suspected. The random SEU cross section of both 4-Gbit DDR3-SDRAM devices is in good agreement with the random SEU cross section of the Samsung 2-Gbit device (Fig. 9). Frequent Device SEFIs are of concern. Not all of these SEFIs can be removed without data loss. Possibly this is not the case for the Hynix 2-Gbit device, but this assessment is based on the very small sample size of only 4 Device SEFIs and has to be supported by more test runs. The calculated error and SEFI event rates, NAND-Flash and DDR3 SDRAM (Tab. IV and Tab. V) are regarded as quite tolerable.

IX. SUMMARY

16/32-Gbit NAND-Flash and 4-Gbit DDR3 SDRAM have been tested. Thinning of DDR3 devices is described. SEU and SEFI cross section diagrams are displayed. Potential removal actions for Persistent SEFIs have been studied. Error rates for EC protected memory for two representative orbits are reported.

X. ACKNOWLEDGEMENT

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