New SEE Test Results of 16/32-Gbit SLC NAND-Flash

Kai Grürmann, Martin Herrmann, Fritz Gliem, Hagen Schmidt, Heikki Kettunen, and Véronique Ferlet-Cavrois

Abstract—16/32-Gbit NAND-Flash memories have been tested under heavy ion irradiation. The cross section and the current waveforms for Destructive Failures and the annealing of hard and soft SEUs are presented.

Index Terms—NAND-Flash, SEE, SEU, MBU, Annealing.

I. INTRODUCTION

NAND-Flash [1] and SDRAM [2] are in use for space mass memories. According to Moore’s law, the storage density of both technologies is still steadily increasing. The contemporary feature size of 25 nm delivers a storage density of about 16 Gbit/cm² for Single Level Cell (SLC) NAND-Flash and of about 4 Gbit/cm² for DDR3 SDRAM.

One objective of our group is to survey the radiation sensitivity of the most recent commercial devices of both technologies. The latest test campaign in April 2012 at RADEF, Jyväskylä, Finland was focused on persistent error/failure phenomena such as Hard SEUs, Device SEFIs of DDR3 SDRAM and Destructive Failures (DF) of NAND-Flash.

Here, we report on the NAND-Flash results.

The array of space mass memories is organized in Word Groups (WG). All $n$ devices of the WG are addressed commonly and are operated in parallel. Typically, the data width of the devices is one byte. Each access writes/reads a word of $n$ bytes/symbols. Typically, the word is protected by Single Symbol Reed-Solomon (SS-RS) coding. In this case, the $n$ bytes of the word are structured into $n-2$ data symbols and 2 parity symbols.

The SS-RS protected WG overcomes the breakdown of one device, provided the WG is free of other errors such as SEUs. Periodic scrubbing is applied to minimize the probability of the coincidence between an extended persistent error pattern in one device and soft SEUs in the other $n-1$ devices. Extended persistent error pattern are produced by a persistent SEFI or a DF. However, scrubbing does not remove hard SEUs. Therefore, the coincidence between an extended error pattern in one device and hard SEUs in the other WG devices is an important scenario for the assessment of the error rate after correction.

The existence of an extended error pattern is detected in the course of the next scrubbing cycle. Power cycling of the WG removes a Device SEFI. In contrast to the volatile SDRAM the stored data are not affected by power cycling. But, in case of a DF the NAND-Flash data have to be saved to another empty WG, similar to SDRAM.

For the memory design, it is important to know how often a NAND-Flash DF occurs. In the same way, the coincidence between a row, column or block SEFI in one device and hard SEUs in the other $n-1$ devices of the WG has to be taken into account.

In this context, the annealing of hard SEUs has to be considered. If all hard SEUs would anneal within some days, then the probability of a coincidence between an extended error pattern and a hard SEU would be rather low compared to non-annealing hard SEUs.

II. TESTED DUTS

Table I shows the tested DUTs.

<table>
<thead>
<tr>
<th>DUT</th>
<th>Size / tested fraction</th>
<th>Part Number</th>
<th>Date Code / Lot Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micron Flash</td>
<td>16 Gbit / 128 Mbit$^a$</td>
<td>MT29F16G08ABACA-WP-IT:C</td>
<td>1122 / BYV7W87.21</td>
</tr>
<tr>
<td>Micron Flash</td>
<td>32 Gbit / 128 Mbit$^a$</td>
<td>MT29F32G08ABAAA-WP-IT:A</td>
<td>1130 / BYZT5C7.21</td>
</tr>
</tbody>
</table>

$^a$128 Mbit = 64 · 64 · 4k · 8 bit

III. TEST FACILITY AND TEST EQUIPMENT

Table II presents the characteristic data of the RADEF ion cocktail.

The basic structure of the NAND-Flash test bed is described in [4].

IV. DESTRUCTIVE FAILURES

Under heavy ion irradiation, NAND-Flash is prone to destructive failures (DF). Typically, erase and write are no longer operable, but read is still functional. In contrast to SEL, the DF is not accompanied by an excessive persistent rise of the...
supply current, but in many cases by a moderate step of the supply current.

The DF event is of statistical nature, just as the SEU and the SEFI events. Fig. 1 shows DF cross section curves from several test campaigns. Open symbols indicate “no DF until the applied fluence”. The state of the art 16-Gbit device delivers \( \sigma_{\text{sat}} \approx 1.0 \cdot 10^{-5} \text{cm}^2 \) and \( LET_{th} \approx 15 \text{ MeV cm}^2/\text{mg} \). The threshold LET of this 25 nm device is lowered in comparison to its 8-Gbit 50 nm predecessor.

The saturation cross section of \( 1.0 \cdot 10^{-5} \text{cm}^2 \) describes a sensitive area of \( 30 \cdot 30 \mu\text{m}^2 \). By masking of the chip surface and also by IR hot spot sensing [5], [6], the sensitive area has been located to be the capacitor-switch cascade of the HV generator and its surroundings. Furthermore, it has been demonstrated that in the DF case, the high voltage drops to a significantly lower value [6]. Presumably, the hit of a high LET ion induces a SEGR of the comparatively thick oxide of the HV switching transistors.

We examined the flux dependence of Samsung 8-Gbit NAND-Flash DFs. From the negative outcome, we conclude that the DF is triggered by a single hit and not by the coincidence of several hits.

Ions of normal incidence - namely those traveling in parallel to the electric field - should be most dangerous with respect to SEGR. The worst case simplification that ions of all directions are as dangerous as those of normal incidence delivers estimates of the mean time until DF occurrence for 1 AU, GCR, 3.7 mm Al: between \( 1.4 \cdot 10^6 \text{ years} \) (8-Gbit and 16-Gbit Micron) and \( 2.5 \cdot 10^5 \text{ years} \) (8-Gbit Samsung). For comparison, the failure rates of commercial memory devices are in the order of 1 FIT, which is equivalent to an average time to failure of \( 1 \cdot 10^9 \text{ h} = 1.2 \cdot 10^5 \text{ years} \). Accordingly, ion induced DFs increase the overall device failure rate by less than a factor of two. In a large space mass memory of e.g. 1000 memory devices, a DF can be expected after more than two hundred and fifty years on average.

At DF occurrence, the program current of the 8-Gbit Samsung device jumps from its plateau amplitude of 40 mA maximum to a continuous current of 80 mA. The DF occurrence is independent of the irregularities of the supply current such as occasional current spikes of several 100 mA or the stepping of the erase/program current pulse. Presumably, these spikes are caused by bus contentions in consequence of a hit induced disturbance of the controlling state machine.

Fig. 2 shows the supply current waveform during the programming of a page. The current raises to a pulse plateau with superimposed needles. These needles reflect the sequence of HV program pulses. Under irradiation, the plateau widens and its amplitude grows, step by step.

V. SEU Annealing

All soft and all hard SEUs are farsifications in \( 0 \rightarrow 1 \) direction. They indicate or fake a loss of FG electrons. Fig. 3 shows the SEU annealing of an earlier 4-Gbit ST NAND-Flash device. SEUs induced by ions of LET between 10 and 32.1 \( \text{MeV cm}^2/\text{mg} \) (Ar, Fe, Kr) show significant annealing. For low LET ions, the annealing is more intensive than for high LET ions.

In case of annealing, charge trapping is the error creating effect. In case of the earlier 4-Gbit device, even at Argon about 90% of the SEUs are due to charge trapping and only the remaining 10% are due to charge loss from the FG. Even at Krypton, about 40% of the SEUs are due to charge trapping.

In contrast, the contemporary 16-Gbit Micron device shows significant annealing only for SEUs induced by very low LET ions (N, \( \text{LET} = 1.8 \text{ MeV cm}^2/\text{mg} \), Fig. 4). SEU generation by

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**TABLE II**

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy [MeV]</th>
<th>LET, Surface MEAS [MeV cm²/mg]</th>
<th>LET, Surface SRIM [MeV cm²/mg]</th>
<th>Range [µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>(^{15}\text{N})(^{4+})</td>
<td>139</td>
<td>1.87</td>
<td>1.83</td>
<td>202</td>
</tr>
<tr>
<td>(^{28}\text{Ne})(^{6+})</td>
<td>186</td>
<td>3.68</td>
<td>3.63</td>
<td>146</td>
</tr>
<tr>
<td>(^{30}\text{Si})(^{8+})</td>
<td>278</td>
<td>6.74</td>
<td>6.40</td>
<td>130</td>
</tr>
<tr>
<td>(^{40}\text{Ar})(^{12+})</td>
<td>372</td>
<td>10.08</td>
<td>10.2</td>
<td>118</td>
</tr>
<tr>
<td>(^{56}\text{Fe})(^{15+})</td>
<td>523</td>
<td>18.84</td>
<td>18.5</td>
<td>97</td>
</tr>
<tr>
<td>(^{82}\text{Kr})(^{22+})</td>
<td>768</td>
<td>30.44</td>
<td>32.2</td>
<td>94</td>
</tr>
<tr>
<td>(^{131}\text{Xe})(^{35+})</td>
<td>1217</td>
<td>54.95</td>
<td>60.0</td>
<td>89</td>
</tr>
</tbody>
</table>

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**Fig. 1.** DF cross section curves

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Fig. 2. Development of the program current window until DF occurrence, (a) soon after irradiation start, (b) midway to the final saturation waveform, (c) the final saturation waveform and (d) after DF occurrence, Samsung 8-Gbit NAND-Flash

Fig. 4. Annealing of SEUs, Micron 16/32-Gbit NAND-Flash

charge trapping is restricted to very low LET. Even at Neon, nearly all SEUs are due to charge loss.

Fig. 5 illustrates the trend that with scaling of the feature size, charge loss dominates over charge trapping. The trapped charge domain is restricted more and more to lower LET.

VI. ANNEALING OF HARD SEUS

Hard SEUs survive a reversing of the cell status by erase-write immediately after beam stop and error verification. We observed annealing of hard SEUs for 16-Gbit NAND-Flash (Fig. 6). The logarithmically scaled bar graph shows the cross section of (i) the total of soft and hard SEUs, (ii) the share of hard SEUs directly after exposure, (iii) the annealing of soft SEUs after 20 days and (iv) the annealing of hard SEUs after 20 days.

The share of hard SEUs increases steadily with LET from $3 \times 10^{-3}$% at Nitrogen to nearly 100% at Xenon. Significant annealing of soft SEUs exists only at Nitrogen. In contrast, typically more than one half of the hard SEUs anneal within 20 days.

Fig. 7 shows the respective cross sections over the linear LET scale. Starting with iron, the cross section per bit exceeds the chip area per bit of $6 \times 10^{-11}$ cm$^2$, which indicates an increasing count of multi-bit SEUs.

All multi-SEUs extend in column direction. Fig. 8 illustrates this for the Micron 16-Gbit device under normal incidence of Xenon ions (LET $\approx 60$ MeV cm$^2$/mg). Soft SEUs are
indicated by small diamonds and hard SEUs by large horizontal bars. In many cases, one or several hard SEUs are accompanied by soft SEUs on one or both sides. Fig. 9 shows the annealing of hard SEUs versus time. For all ion species except Xenon we get substantial annealing, more pronounced for lower LET ions. Xenon, Iron and Neon induced hard SEUs show some reverse annealing for some ten minutes after exposure.

An erase-write operation after 80 days (Fig. 4) delivered a complete annealing of the heavy ion induced hard SEUs. Only a fraction of the nitrogen induced hard SEUs survived, but disappeared within the following 30 erase/write cycles. One hundred days after irradiation, the read of the Xenon-exposed DUT delivered 95% of the initial count of hard SEUs. An erase-write-read reduced this count to 55%. But then, the count of hard errors increased again with time as depicted in Fig. 10.

VII. DISCUSSION

The stepping of the program current (Fig. 2) reflects a closed loop controlled adaptation of the count of high voltage pulses. We assume that the HV leakage current increases by
ion induced defects, possibly by micro latch ups [6]. The associated reduction of the pulse tunnel current is compensated by more programming pulses. After a given number of compensation steps, this process comes to an end, mostly before DF occurrence, but the converse situation happens as well. The mean time until DF is larger than the mean time until the freeze of the adaptation of the program pulse sequence.

The fact that a further degradation of the program pulse voltage can not be compensated anymore by an increased count of program pulses raises some concern about the long term data retention. The decreasing amount of injected FG charge should result in a reduced data retention time. In consequence, for applications with large data storage time, the usability of the device should be determined rather by the freezing of the program pulse window than by the DF occurrence. This issue requires further investigation.

Presumably, the center of the hard error pattern given in Fig. 8 reflects the shortest distance between the transistor string and the ion track. The SEUs always affect the same bit position of the same byte of subsequent pages. Physically, in the string of concatenated transistors, the channels of adjacent transistors can not be depleted by the lowered word line voltage.

This seems to indicate that the hard SEUs are caused by a large trapped charge, which can not be compensated by the negative charge of a single write cycle, and which anneals over time.

The write operation charges all FGs including those with impaired insulation. The starting count of hard SEUs reflects cells which are in erroneous state (i) because of still not sufficiently removed trapped holes, or (ii) because of an immediate loss of FG electrons due to a leakage current of more than some ten electrons per second.

The increasing count of hard SEUs (Fig. 10) reflects the discharge of less impaired FG structures by an even smaller leakage current. If, for example, an additional SEU is created by the loss of 360 electrons in one hour, then the leakage amounts to only one electron per second or \(1.6 \times 10^{-4} \text{ fA}\).

The “reverse annealing” of the heavier ion curves in Fig. 9 can be explained by the superposition of the increasing count of “resistive” hard SEUs and the decreasing count of “charge trapping” SEUs. The steady loss of FG electrons makes more and more “resistive” hard SEUs visible.

Persistent hard errors accumulate over the mission time. Their detrimental effect on the error rate increases steadily. In contrast, soft SEUs accumulate only over the data storage time, which is only of some days in many cases. Hard errors survive scrubbing and can therefore be more harmful.

REFERENCES