New SEE and TID Test Results for 2-Gbit and 4-Gbit DDR3 SDRAM Devices

Martin Herrmann, Kai Grürmann, Fritz Gliem, Hagen Schmidt, Michele Muschitiello, and Véronique Ferlet-Cavrois

Abstract

Different 2-Gbit and 4-Gbit DDR3 SDRAM devices have been tested. Under $^{60}$Co, some of them showed a peculiar error pattern. Under heavy ions, none of the tested types displayed any latch-up.

Index Terms

DDR3, SDRAM, TID, SEE

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M. Herrmann is with IDA, Institute of Computer and Network Engineering, Technische Universität Braunschweig, P. O. Box 3329, D-38106 Braunschweig, Germany (phone: +49 531 391 9679, fax: +49 531 391 4587, email: mherrmann@ida.ing.tu-bs.de).

K. Grürmann and F. Gliem are with IDA, Institute of Computer and Network Engineering, Technische Universität Braunschweig, P.O.Box 3329, D-38106 Braunschweig, Germany.

H. Schmidt is with Astrium GmbH, D-88039 Friedrichshafen, Germany.

M. Muschitiello and V. Ferlet-Cavrois are with the European Space Agency, ESA-ESTEC, Keplerlaan 1, 2200AG Noordwijk, Netherlands.
I. INTRODUCTION

SDRAM devices [1] are relevant for space applications – in particular for spacecrafts that will encounter a high total dose, like ESA’s upcoming JUICE mission [2].

DDR3 SDRAM devices have been shown to be still functional after more than 400 krads with an error density of less than $10^{-6}$ after 300 krads [12]. However, we encountered a peculiar error pattern, the band error pattern, starting at 150 krads, for 4-Gbit DDR3 devices from Samsung. This error pattern can only be mitigated by a tailored memory controller, which may not be feasible for some applications.

SEU and SEFI cross sections are known from previous test campaigns [9] [10] [11]. The sensitivity to single-event latch-up (SEL), however, is not known so far.

In order to assess these questions, we performed two test campaigns, one SEE test and one TID test.

The SEE test was performed at Texas A&M University in December 2012. Its goal was to determine the single-event latch-up (SEL) response of DDR3 SDRAM devices, as well as to validate and supplement SEU and SEFI data gathered at previous tests.

The TID test was performed at ESTEC in March 2013. Its goal was to supplement the data gathered in our previous in-situ test of 4-Gbit Samsung devices in October, 2013 [12] by testing more devices from a larger spectrum of manufacturers. Specifically, we examined these new devices for the band error pattern.

II. MEMORY DEVICES

In the SEE campaign, we tested 4 different parts from 2 manufacturers, as shown in table I. All of the devices were opened. They were thinned to either 60 µm (for comparison with RADEF tests) or 200 µm, with the exception of the 2-Gbit Samsung devices, which have an original thickness of 200 µm. The thinning process is described in [10].

In the TID campaign, we tested 9 parts from 5 manufacturers, as shown in table II. Some of the Hynix devices were soldered to an SODIMM [4] module. Other than that, none of the devices were prepared in any way, such as opening or thinning.

In this test, all devices were unbiased during irradiation. They were mounted in a plastic frame with the balls of the devices placed on conductive foam (figure 1) and shielded against electrons with a 3 mm sheet of acrylic glass as well as a 3 mm aluminum sheet.

For the Samsung 2-Gbit parts, two die revisions were tested: die revision D is produced in 35 nm feature size, while die revision B is produced in the previous generation ($\approx$ 50 nm) feature size. For the Nanya 2-Gbit parts, two die revisions were tested: die revision G is produced in 42 nm feature size, while die revision B is produced in 50 nm feature size.

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V. SEE TEST PROCEDURES AND TEST RESULTS

A. Comparison with previous results

Figures 2 and 3 show the results of the 12/2012 TAMU campaign alongside the results from former test campaigns at RADEF, Jyväskylä, Finland [10] [11]. The figures show the SEU and device SEFI cross section, respectively, for Samsung 4 Gbit without software conditioning.

The SEU cross section from the TAMU test campaign is about one order of magnitude lower than the RADEF campaigns (figure 2). This may have been caused by a difference in DUT temperature; the tests at TAMU were performed in air at a temperature of less than 80 °C. The tests at RADEF, on the other hand, were performed in vacuum. The temperature of the DUT in vacuum is not known, but based on the power dissipation of approximately 150 mW during write operation, it is estimated to be about 60 °C.

For the device SEFI cross sections (figure 3), the TAMU values and the RADEF values fit within the error margin resulting from the low number of observed SEFIs.

B. Single-event latch-up

In order to test for single-event latch-up (SEL) events, five 4-Gbit DUTs (two from Samsung and three from Hynix) were heated to 80 °C using a heat gun and irradiated with $10^7$ cm$^{-2}$ of 61.1 MeV cm$^2$/mg xenon ions while operating them in write/read mode.

No latch-up events were observed for any of the devices at the given LET.

All SEL tests were performed at normal incidence because our test bed does not allow tilting the DUTs at this time.

C. Current

For the single-event latch-up test (section V-B), the current was logged with a sampling rate of 1 Hz before, during, and after irradiation. This sections gives a summary of the results. The current values (idle, read and write) without irradiation are called the baseline current values.

The main results are:

- Heating a device does not significantly change the operating current.
- Under irradiation, the current (both idle and operating) is sometimes increased for some time, e.g. 1 minute. It then returns to a lower value or the baseline value.
- After the end of the irradiation, the idle current drops to its baseline value quickly (within seconds). No permanent current increase was observed.
- The current increase may be severe. For example, an idle current of $\approx 200$ mA has been observed, compared to a baseline idle current of $\approx 20$ mA.

Current plots will be shown in the final paper.

VI. TID TEST PROCEDURES AND TEST RESULTS

A. Band error pattern description

Under TID testing, a band error pattern has been observed [12], consisting of a high number of errors which are likely triggered by keeping a page active for an extended period of time (within the constraints given by the specification [3]). Keeping one page open causes errors in several regions of a device that has been damaged by radiation. This pattern depends heavily on the mode of operation.

The band error pattern is exacerbated by the fact that Xilinx’ DDR3 PHY, driving the DDR3 devices, requires a periodic read (PRD) operation [5]. This operation repeatedly activates that last page that had been accessed during a test run, which is therefore active for a long time.

B. Test procedure

The unbiased devices were irradiated with $\approx 376$ krad (silicon) at a dose rate of $\approx 2.3$ krad/h (as opposed to $\approx 4.3$ krad/h for the previous in-situ test [12]). The balls of the devices were connected to each other through conductive foam.

After the devices had been shipped back after the end of the irradiation, various tests were performed in our laboratory.

In order to reduce the active time of the last page accessed in the test, the test bed can be configured to precharge the page as soon as possible (precharge after periodic read (PRD)).

In order to cause other rows to be kept active for an extended time, the test bed can be configured to perform intermittent operation. This is similar to read operation, but includes additional pauses which keep the current row active.
Figure 4: Error density (number of errors divided by device capacity) measured at room temperature after 376 krad. Each point in the graph corresponds to one tested sample.

Subsequently reading the data from the DUT in continuous operation (without rewriting) typically results in a higher number of errors.

C. Results at room temperature

First, a subset of the irradiated devices were tested at room temperature after 376 krad:

- The band error pattern was observed for 4-Gbit Samsung as in the October 2012 in-situ test and also for the 2-Gbit Samsung (revision D) devices. In the “worst” affected rows, about 5% of all cells contained the wrong value.
- There were no errors for 2-Gbit Micron and 2-Gbit Nanya devices, with the exception of one single error each in one Micron device (out of the 6 devices tested) and one Nanya device (out of the 12 devices tested). These errors were 1-to-0 transitions in the second to last page (page address 0x7ffe), suggesting that it constitutes a very weak band error pattern.
- There were no errors at all for 4-Gbit Hynix, 4-Gbit Elpida, 2-Gbit Samsung (revision B), 2-Gbit Micron, and 2-Gbit Nanya devices.

The 4-Gbit Samsung devices had a consistent number of bit errors, as shown in figure 4 (note that only devices from one lot were available for testing, so the lot-to-lot variation remains unknown). The 2-Gbit Samsung devices, on the other hand, showed considerable device-to-device and lot-to-lot variation.

D. Results at elevated temperature

Since errors are more pronounced at higher temperature [12], the devices were operated at elevated temperature. At least 3 samples of each device type were operated at 85 °C, the maximum temperature that is allowed for all of the devices. First, several write and read operations were performed without and, in case of errors, with precharge after periodic read. After that, intermittent operation was performed on the first half of the device and the whole device was read again (an example where intermittent operation has a strong effect is shown in figure 5a).

At 85 °C, and in contrast to room temperature, the band error pattern was observed for many devices, not just for the 4-Gbit Samsung device (table IV).

The band error pattern consists of several error regions with different error intensity, as described in detail in [12] – in particular, four regions consisting of 512 pages each (class 2 in [12]) and two single pages with a very high error density close to the end of the device (class 3).

For a weak band error pattern, all but the errors of class 3 are so weak that they cannot be recognized. A very weak band error pattern consists of few isolated errors in the two pages of error class 3. Examples for the error intensities are shown in figure 5b.

Precharge after periodic read typically reduces the band error pattern significantly. If the band error pattern is weak in the first place, it may be reduced to the point of disappearing completely. An effect on the random errors could not be observed.

Note that all three 2-Gbit Samsung (revision B) devices did not show any errors at all, even after intermittent operation at 85 °C, in very contrast to the 4-Gbit and 2-Gbit (revision D) devices from the same manufacturer.

In an additional test, one of the tested 2-Gbit Micron devices contained more random errors and the other showed a stronger band error pattern. Another 2-Gbit Micron device showed random errors in a pronounced gradient pattern (figure 5c).

VII. DISCUSSION

A. SEE tests

For the tested Samsung and Hynix devices, no latch-up was observed. All of these devices showed a substantial increase in operating current. The current returned to its pre-irradiation value immediately after the end of the irradiation, indicating that the current increase is a transient effect and probably flux dependent.

The current measurements were performed at a comparatively high LET and flux and may not be representative for low flux space environments.

B. TID tests

The band error pattern is exhibited by several devices, although typically much weaker than for the 4-Gbit Samsung device.

The 2-Gbit Samsung (revision D) device behaves very similarly to the 4-Gbit Samsung device, which is manufactured with the same feature size. In particular, the band error pattern is almost identical. In very contrast, the 2-Gbit Samsung (revision B) device, manufactured with a larger feature size, behaves differently: it seems much less susceptible to errors. Significant lot-to-lot and device-to-device variation have been observed for some devices, but not for others.

As detailed in [12], the band error pattern can be reduced significantly by operational measures; however, this may not be possible with a stock memory controller but may require a tailored controller design.

VIII. FUTURE WORK

We are planning to perform a SEL test at 60° incidence. For future tests, we plan to perform current measurement with a higher sample rate at lower flux, and also for lower LET.

For TID, we are planning another unbiased test with more 4-Gbit devices from other manufacturers, and another in-situ test with the two best-suited device types.
(a) after intermittent operation in the first half of the device, a high number of errors is generated. 2-Gbit Samsung, revision D, after 376 krad

(b) Examples of error intensities: few, significant and severe random errors; very weak, weak and strong band error pattern. Various devices after 376 krad

(c) Gradient pattern and weak band error pattern. 2-Gbit Micron, after 376 krad.

Figure 5: Error maps. A blue symbol indicates a 32-bit word with a single-bit error. A purple symbol indicates a word with 2 or 3 bit errors, and a red symbol indicates a word with 4 or more bit errors. All at 85°C.

Table IV: Test results at 85°C (ordered by band error pattern severity)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Capacity</th>
<th>Revision</th>
<th>Samples</th>
<th>Lots</th>
<th>Random errors</th>
<th>Band error pattern (BEP)</th>
<th>Precharge after periodic read</th>
<th>Intermittent operation</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Samsung</td>
<td>4 Gbit</td>
<td></td>
<td></td>
<td>8</td>
<td>1 Severe</td>
<td>Strong</td>
<td>Reduces BEP</td>
<td>More errors</td>
<td>See [12]</td>
</tr>
<tr>
<td>Samsung</td>
<td>2 Gbit</td>
<td>D</td>
<td>4</td>
<td>2</td>
<td>Severe</td>
<td>Strong</td>
<td>Reduces BEP</td>
<td>More errors</td>
<td></td>
</tr>
<tr>
<td>Micron</td>
<td>2 Gbit</td>
<td></td>
<td>4</td>
<td>2</td>
<td>Significant/severe</td>
<td>Weak</td>
<td>Removes BEP</td>
<td>No effect</td>
<td></td>
</tr>
<tr>
<td>Hynix</td>
<td>2 Gbit</td>
<td></td>
<td>3</td>
<td>1</td>
<td>Few</td>
<td>Weak/very weak</td>
<td>Removes BEP</td>
<td>No effect</td>
<td></td>
</tr>
<tr>
<td>Nanya</td>
<td>2 Gbit</td>
<td>B</td>
<td>3</td>
<td>3</td>
<td>Significant</td>
<td>Very weak</td>
<td>No effect</td>
<td>No effect</td>
<td></td>
</tr>
<tr>
<td>Nanya</td>
<td>2 Gbit</td>
<td>G</td>
<td>3</td>
<td>1</td>
<td>Few</td>
<td>None</td>
<td>No effect</td>
<td>No effect</td>
<td></td>
</tr>
<tr>
<td>Hynix</td>
<td>4 Gbit</td>
<td></td>
<td>19</td>
<td>3</td>
<td>Few</td>
<td>None</td>
<td>No effect</td>
<td>No effect</td>
<td></td>
</tr>
<tr>
<td>Elpida</td>
<td>4 Gbit</td>
<td></td>
<td>3</td>
<td>1</td>
<td>None</td>
<td>None</td>
<td>No effect</td>
<td>No effect</td>
<td></td>
</tr>
<tr>
<td>Samsung</td>
<td>2 Gbit</td>
<td>B</td>
<td>3</td>
<td>1</td>
<td>None</td>
<td>None</td>
<td>No effect</td>
<td>No effect</td>
<td>cf. rev. D!</td>
</tr>
</tbody>
</table>

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