ARCS 2009

March 10-13, 2009, Delft, The Netherlands
http://www.ida.ing.tu-bs.de/arcs09/

WORKSHOP ON

MANY-CORES

The advancement from single core to multi-core processors is expected to continue resulting in many-core chips with up to hundreds or thousands of cores per chip. This progress raises new important questions concerning new programming paradigms, future system architectures (shared memory, distributed shared memory or message passing), the kind of cores that will be used (heterogeneous or homogeneous cores), reliability issues, and how to use the enormous chip-level parallelism.

This workshop should consider software and hardware directions in which many-core architectures may be heading and look at the impact on parallel programming and scientific computing. Besides new research work in the area of many-core architectures also work-in-progress presentations are encouraged.

Workshop topics for many-cores

focus on but are not limited to

- Interconnection architectures like NoC
- Processor core architectures
- Many-cores in embedded systems
- Fault detection
- Real-time aspects
- Special operating system topics
- Virtualization techniques
- System aspects
- Adaptivity and reliability
- Self-configuration and auto-tuning
- Programming tools and techniques
- Programming models and languages
- Performance modelling and prediction
- Parallelization experience reports

Important dates:

Submission until	Dec. 14, 2008
Notification of acceptance	Jan. 16, 2009
Final version until	Jan. 26, 2009

Submission of papers

Papers must be submitted in PDF format in English. The papers should have a maximum of 10 pages and be formatted in the VDE publisher style:
http://www.vde-verlag.de/engl/tagunge.html

Please submit papers to Sascha Uhrig:
<uhrig@informatik.uni-augsburg.de>

Workshop chairs

Sascha Uhrig, University of Augsburg
Theo Ungerer, University of Augsburg

Program committee

Nader Bagherzadeh, Univ. of California, Irvine, USA
Arndt Bode, TU München, Germany
Uwe Brinkschulte, TU Karlsruhe, Germany
Francisco Cazorla, UPC Barcelona, Spain
Glenn Farrall, Infineon, Bristol, GB
Michael Gerndt, TU München, Germany
Andreas Herkersdorf, TU München, Germany
Christian Hochberger, TU Dresden, Germany
Wolfgang Karl, TU Karlsruhe, Germany
Christian Lengauer, University of Passau, Germany
Thomas Rauber, University of Bayreuth, Germany
Gudula Rünger, TU Chemnitz, Germany
Pascal Sainrat, UPS Toulouse, France
Jan Staschulat, NXP, The Netherlands
Walter Tichy, TU Karlsruhe, Germany
Pedro Trancoso, University of Cyprus