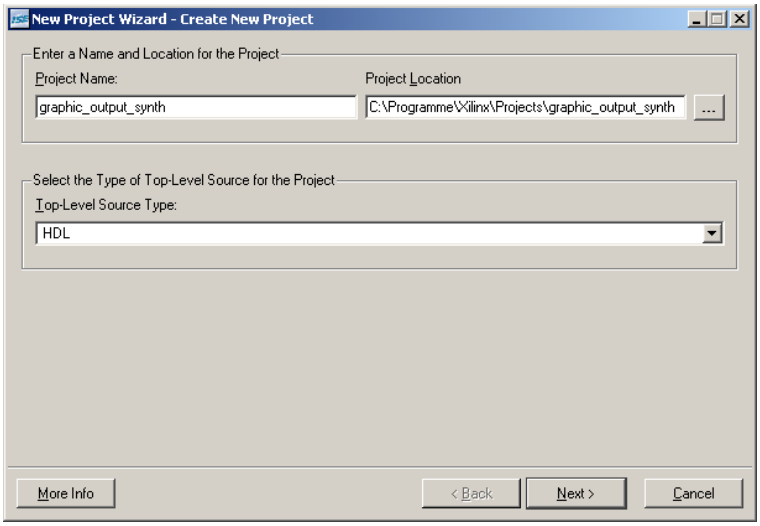
Computer aided design of digital circuits

How to create a new project with the Xilinx ISE tools:

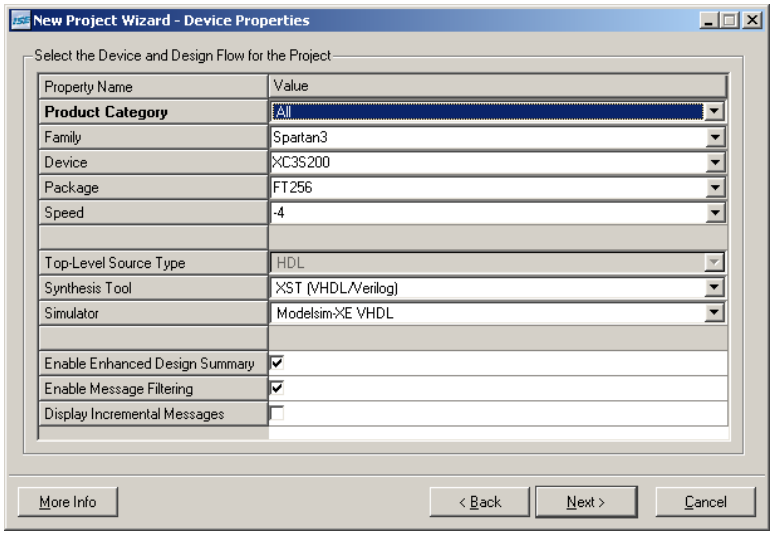
Start the Xilinx ISE by typing *ise* in the console.
The ISE tools will start with the last opened project.

If no project has been created yet, click on F*ile => New Project.*

Enter a project name and, if necessary, change the path.



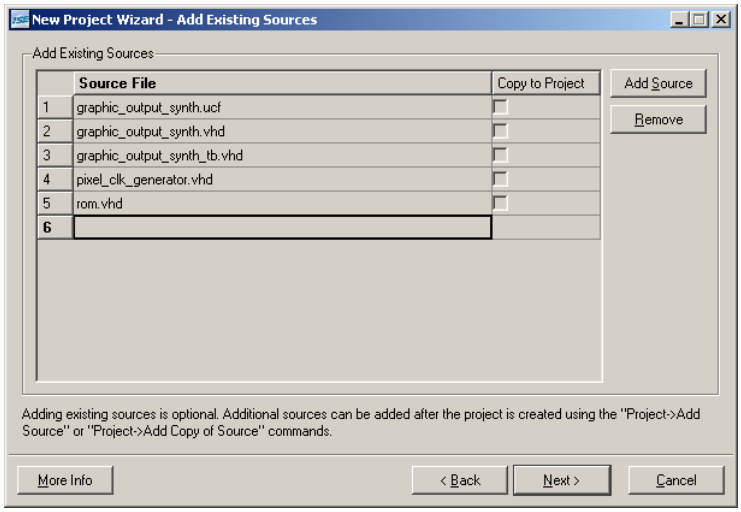
Enter all data according to the picture and click on *Next.*



In the *Create New Source* window click on *Next.*

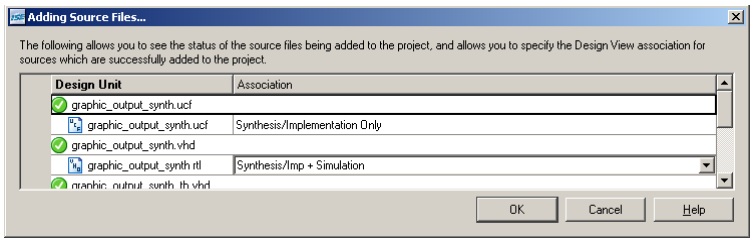
In the next window click on *Add Source* and select all files you want to add to the project (Important: DO NOT FORGET TO ADD THE .ucf FILE. IT CONTAINS THE PIN ASSIGNMENTS FOR THE FPGA). You can disable the C*opy to Project* option, so you don't have

to replace the file in the project directory once you changed it in its destination directory. After you added all files click on *Next*. You can add files later, if you want.

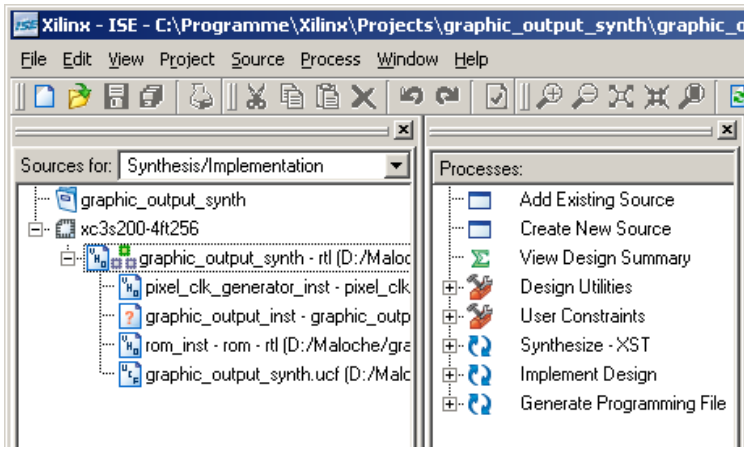


In the *Project Summary* click on *Finish*.

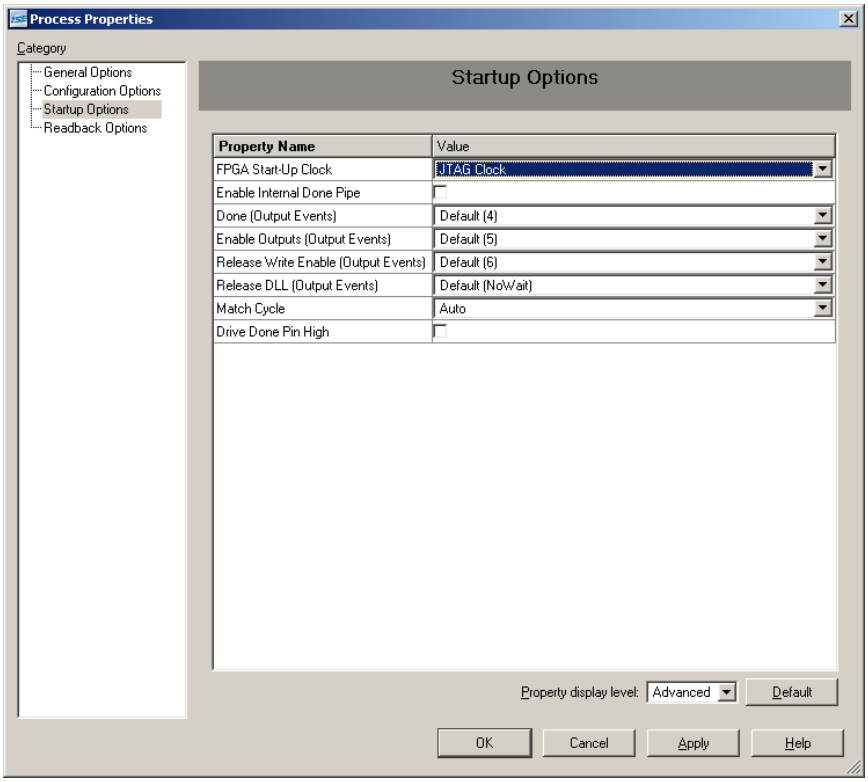
In the next window you can choose whether a file can be used during simulation, synthesis or both. In most cases the selected options are correct. So just click on *OK*.



Now you see the Project Navigator window with all files (in fact you see the entities or instances of entities). Missing entities are marked with a question mark. The top entity is marked with three little squares. In most cases, the top entity is correctly chosen by the ISE. If you have to change it, click on the entity you want to move to the top and right-click on it. Then select *Set as Top Module*. To add files, right click in the Project Navigator and select either *Add Source...* for existing files or *New Source...* to create a new source file.



Once you added all files, you have to right click on *Generate Programming File* in the Processes window and select *Properties*. Select *Startup Options*, and change *FPGA Start-Up Clock* to *JTAG Clock*.



To generate a programming file, simply double-click on *Generate Programming File*, or you can run all three necessary steps one after another by clicking on them separately. At the end you should have a file named [*project name*].bit in your project directory. This file is then used to program the FPGA.