A Reconfigurable Hardware Platform for Digital Real-Time Signal Processing in Television Studios

Kersten Henriss, Peter Rüffer, Rolf Ernst

Institut für Datenverarbeitungsanlagen
Technische Universität Braunschweig
Hans-Sommer-Straße 66, 38106 Braunschweig, Germany
{K.Henriss, P.Rueffer, R.Ernst}@tu-bs.de

Sieghard Hasenzahl

Philips Digital Video Systems
Brunnenweg 9, 64331 Weiterstadt, Germany
Sieghard.Hasenzahl@philips.com

Abstract

By the continuous increase of speed and capacity of field programmable gate arrays (FPGAs) it becomes possible not only to process digital video data by FPGAs in real-time but also to implement the logic of complex video algorithms in one FPGA. For television (TV) studios the adherence to the real-time constraint is a mandatory requirement. Besides the reconfigurability of FPGAs allows the execution of different algorithms on the same hardware.

With the reconfigurable hardware platform introduced in this contribution different video standards including high definition television (HDTV) can be processed in real-time. To realize a system with many complex video applications the platforms can be cascaded.

1 Introduction

Professional TV studios are characterized by processing, storing and transmitting of digital video data. These tasks require a high data bandwidth and consume a great amount of computing power. Additionally they have to be processed within a fixed time slot determined by the television scanning standards. Nowadays TV studios have to operate a multitute of different video standards ranging from standard CCIR 601 [1] (data rate 270 Mbit/s) up to future HDTV standards like SMPTE 296M [2] and SMPTE 274M [3] (data rate 1485 Mbit/s). In the following, this fixed time slot constraint will be named as real-time.

To meet real-time processing requirements most of the professional TV equipment consist of dedicated hardware. As a drawback, dedicated hardware is less flexible with respect to changes and scalability. Even minor modifications lead to cost intensive redesigns. On the other hand, pure software solutions running on high-end workstations have branched out into the market of (offline) audio-visual movie productions. In comparison with dedicated hardware realizations a pure software implementation is characterized by a nearly unlimited flexibility. The performance of software solutions, however, is either far below professional video standard requirements or too expensive for the market.

In the recent years FPGAs have shown large progresses concerning (a) the increasing number of logic cells and memory and (b) the increasing system clock frequency. Moreover, FPGA programmability has reached a high level of sophistication. Comfortable FPGA design tools using CAD technologies have decreased the design time and thus the time to market. The ability to reconfigure FPGAs has not only removed the unflexibility of a pure fixed wired hardware solution but also enables us to implement a task optimized processing unit with a FPGA core which complies with TV studio system real-time constraints.

2 The Processing Unit

Optimization for different tasks is obtained by reprogramming the FPGA according to the desired algorithms before the start of a video production. Therefore our implemented real-time processing unit (PU) acts as a universal platform which can be adjusted to different tasks within a TV studio (first CCIR 601 compliant, now HTDV SMPTE 274M).

The block diagram of figure 1 shows the structure of the PU. The main components of the PU are

1. a reconfigurable FPGA (first Xilinx XC4085, now Xilinx Virtex XCV600),
2. an (arbitrary) digital signal processor subsystem,
3. a cost-efficient image storage using inexpensive Synchronous Dynamic RAMs (SDRAMs) and
4. an (optional) arithmetic expansion (FPGA or dedicated signal processing unit).

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The core of the PU is realized by the FPGA which is subdivided into (a) a Video Interface with two independent 20-bit parallel video input channels and two synchronous 20-bit parallel video output channels for SMPTE 274M (10-bit for CCIR 601), (b) a SDRAM Interface to control SDRAM access with a data bandwith of 324 MByte/s (XC4085) and 594 MByte/s (XCV600), (c) a Digital Signal Processor (DSP) Interface as a connection to a DSP system which may serve as a connection to a host system, (d) an Arithmetic Interface which provides FPGA on chip signal processing capability and may interlink the FPGA and an optional arithmetic expansion or another PU and (e) a Configuration Interface to configure the FPGA by the DSP or via JTAG.

The FPGA structure permits quasi concurrent real-time memory access for the two video input channels, the two video output channels, the DSP and the arithmetic interface. This access is a substantial gain of the PU structure compared to an earlier implementation [4].

The data signals of the video standard CCIR 601 are carried in 10-bit samples at 27 MHz. Using a 64-bit SDRAM module at a system clock frequency of 40.5 MHz nine memory accesses per sample are possible within the fixed sample time slot. The 20-bit (2 samples) video data words of SMPTE 274M are transmitted at 74.25 MHz. With a 64-bit SDRAM module operating at the same frequency there are three possible memory accesses per word. Because the clock signals of SDRAM, video and DSP are independent of each other by applying FIFOs, the number of memory accesses can be increased linear with the clock frequency of the SDRAM.

3 Conclusion and future work

Quite different algorithms can be easily implemented by reconfigure the FPGA. The parameters needed for some algorithms (e.g. move of the output frame, FIR filter) can be calculated by the DSP and transmitted to the FPGA.

For the next generation of the PU a Xilinx Virtex-E FPGA and Double Data Rate (DDR) SDRAM will be applied. This application will increase the memory data bandwidth and therefore the number of possible memory accesses.

References

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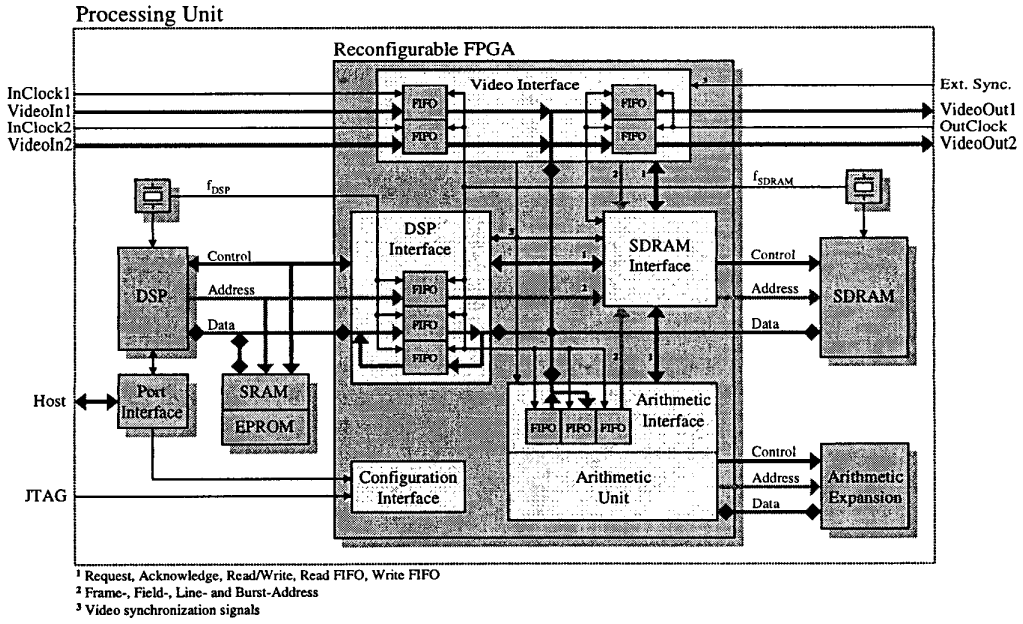

Figure 1. Architecture of the reconfigurable Processing Unit