Radiation Evaluation of Samsung 8 Gbit Flash Memories for Space Application

H. Schmidt, K. Grürmann, D. Walter, F. Gliem, H. Michalik

Institut für Datentechnik und Kommunikationsnetze
TU Braunschweig

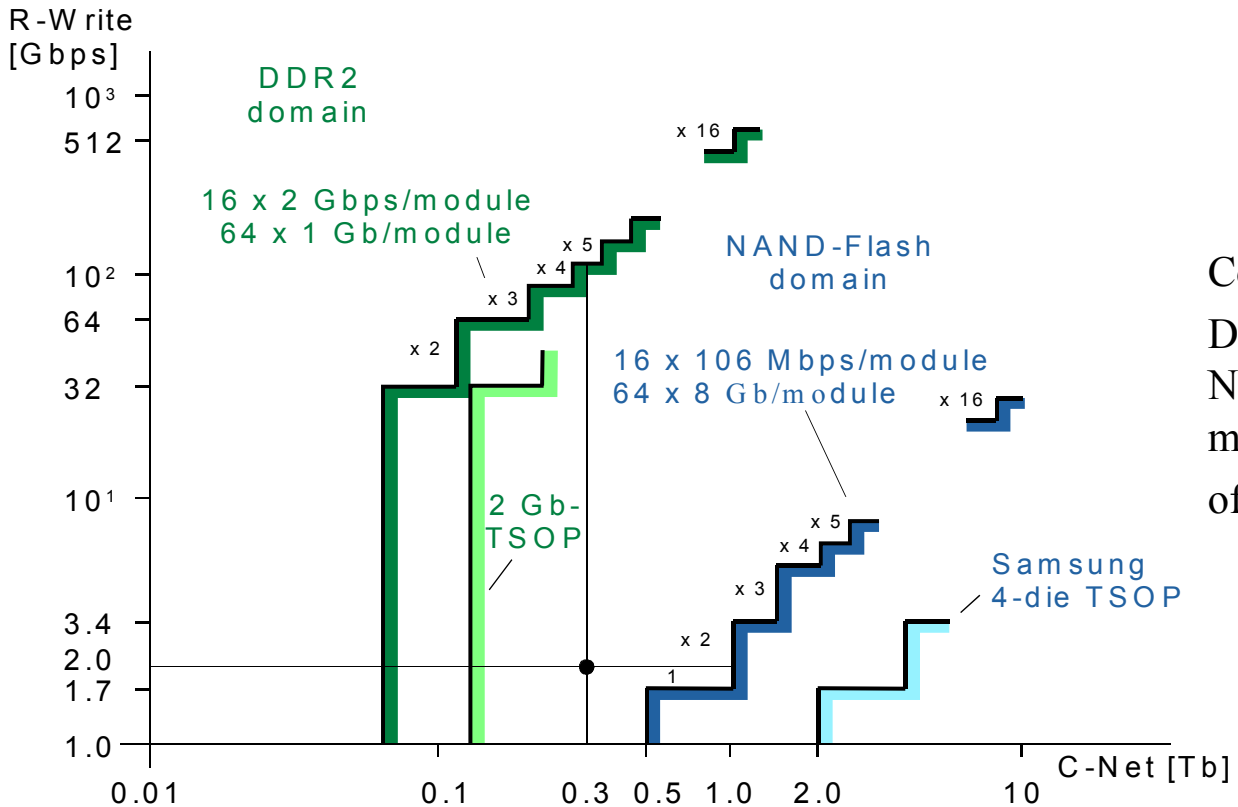
Flash versus SDRAM

Flash Features:

- \+ Non-volatile
- \+ High capacity, 8 Gbit per die
- − Slow access to pages
- − Wear Out after > 10^5 writes / block

SDRAM Features:

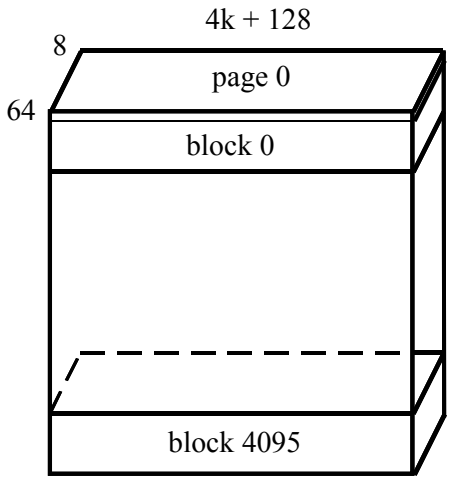
- − Volatile
- − 2 Gbit per die
- \+ Fast access to bytes
- \+ No Wear Out



Comparison between DDR2 SDRAM and NAND flash mass memory modules of equal size and mass

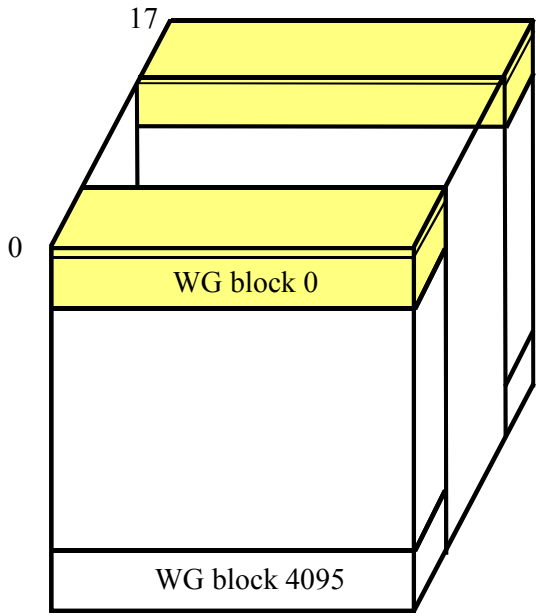
Word Group of 16 Data Bytes + 2 Parity Bytes for Reed-Solomon Single Symbol EC

The storage array of mass memory modules is composed of e.g. 8 Word Groups (WG) of e. g. 16+2 devices, each. Reed Solomon Single Byte Error Correction is capable to correct one faulty byte (= device) out of (16+2) bytes.



Device Organization

(4k + 128) byte = 1 page
64 pages = 1 block
4 k blocks = 1 device



WG Organization

1 WG word = 16 + 2 bytes
(4k + 128) WG words = 1 WG page
64 WG pages = 1 WG block
4k WG blocks = 1 WG = 18 devices

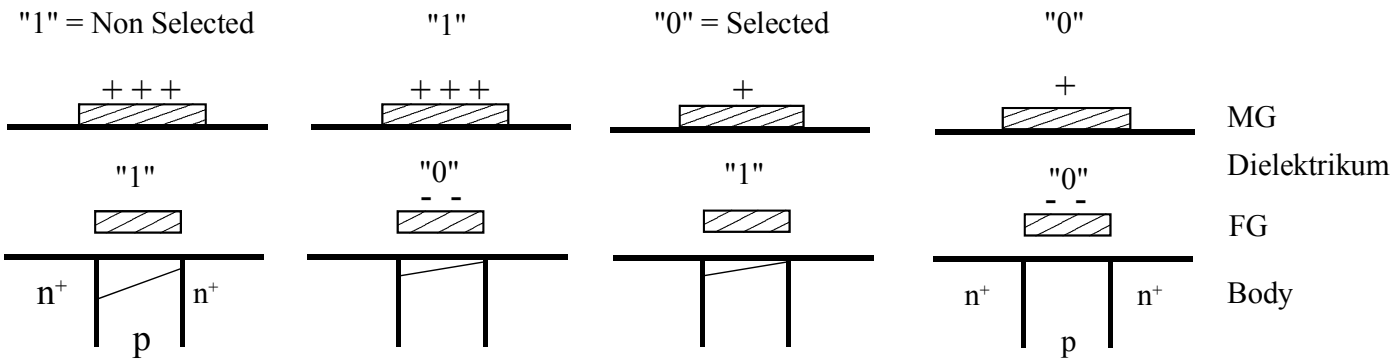
Relevance of Device Errors in Case of Single Symbol EC

Type of Device Error / Failure:	Spoiled Data Words:
≥ 2 single bytes of the same Word	1
1 page + n bytes of the same WG Page	n
1 column + n bytes of the same WG Column	n
1 block + n bytes of the same WG Block	n
1 device + n bytes of the same WG	n
1 page + n pages of the same WG Page	4k
1 page + n columns of the same WG	n
• • •	
1 device + n bytes of the same WG	n
1 device + n pages of the same WG	n · 4k
1 device + n columns of the same WG	n · 64
1 device + n blocks of the same WG	n · 4k · 64
1 device + n devices of the same WG	n · 4k · 64 · 4k = 1G

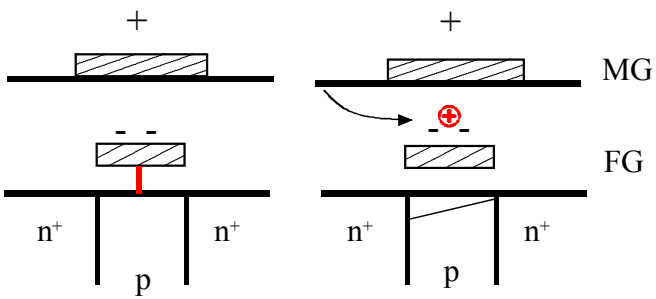
Typically "Flash Write" fails before "Flash Read".
Data of "no more writable" devices still can be retrieved and swapped to other memory locations.

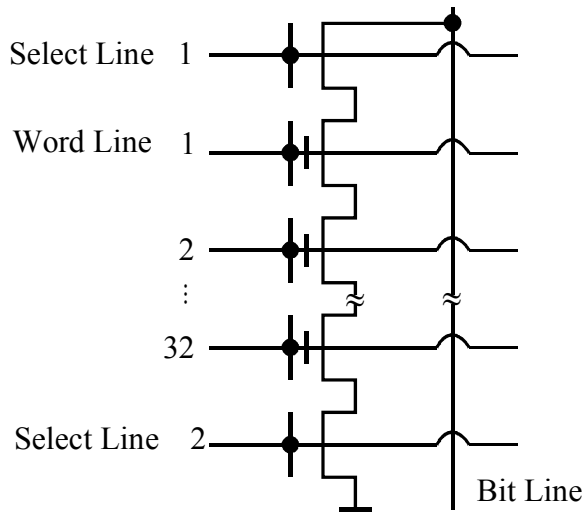
Classification of device errors and error class individual cross sections are needed to predict the memory performance in space (e.g. BER).

Basic Cell Operation, Basic Cell Error Mechanisms, NAND Flash Structure

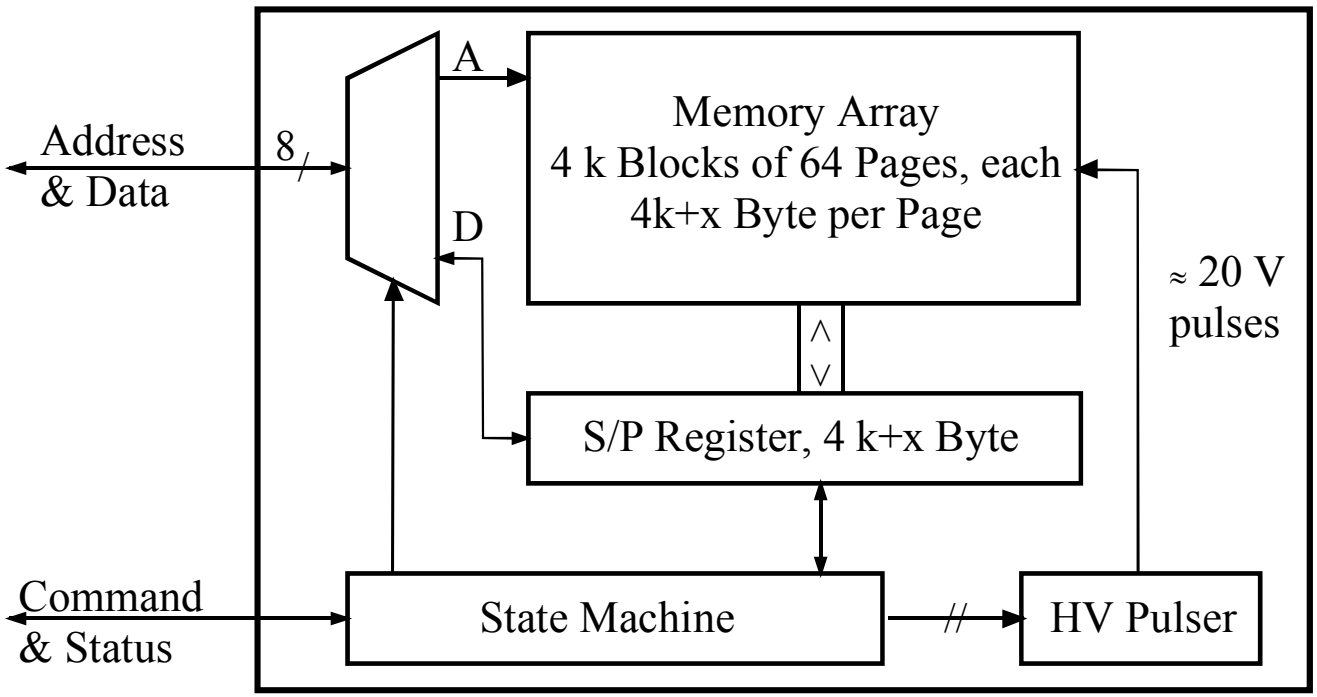


WL	Data	BL
1	1	0
1	0	0
0	1	0
0	0	1





Functional Block Diagram of 8 Gbit NAND Flash Memory Devices



Samsung x = 128
Micron x = 218

Basic Flash Memory Operations

Program: Pagewise
Serial byte transfer user → 4224 byte data register DR,
parallel programming of "0" by pulsed electron tunneling,
page program time:
4224 byte · 30 ns/byte + < 700 µs ≈ < 850 µs

Read: Pagewise
Status of 4224 · 8 selected transistors → DR,
serial byte transfer DR → user,
page read time:
4224 byte · 30 ns/byte + 25 µs ≈ 150 µs

Erase: Blockwise → "1"
Parallel discharging of 4224 · 8 · 64 storage cells
by pulsed electron tunneling,
block erase time: < 2 ms

Complexity of Flash Memory Operations

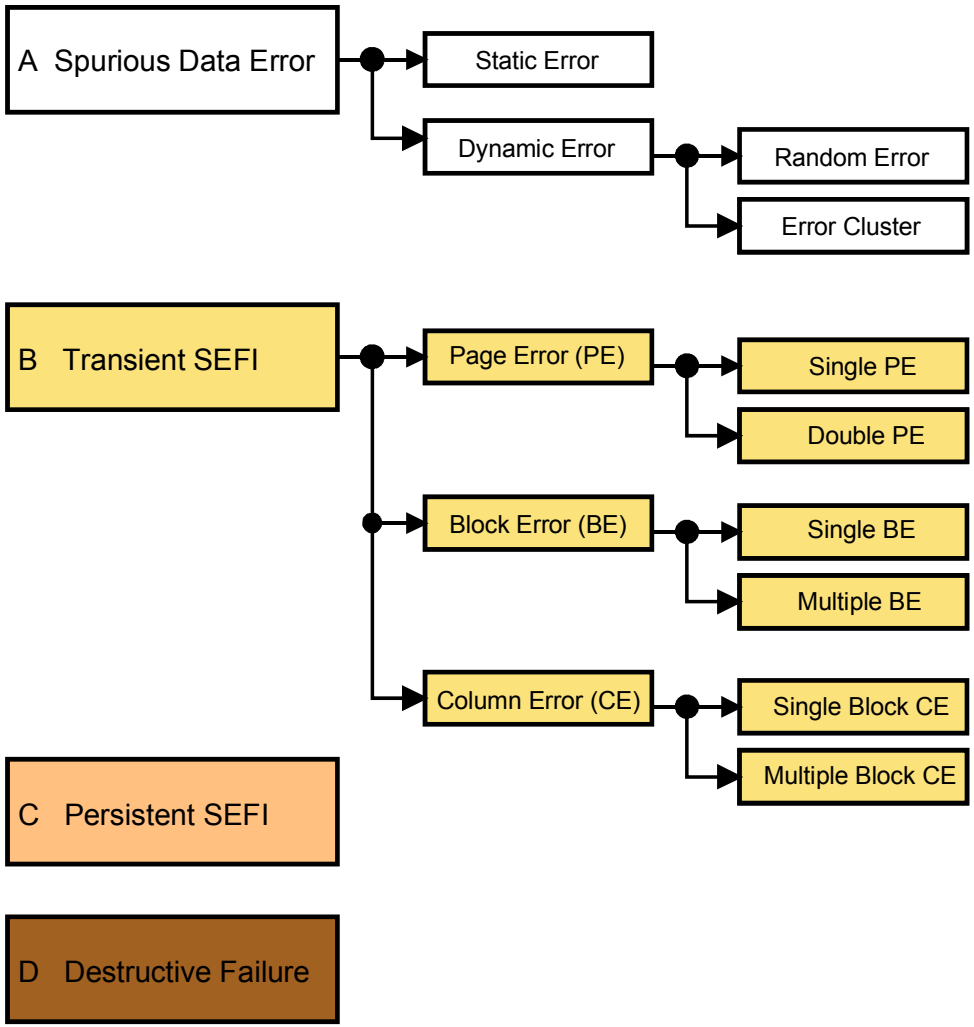
Device internal voltage generator delivers “high voltage” pulses of about 20 V to achieve sufficient electrical field strength (≈ 20 MeV/cm) across the thin oxide (< 10 nm) between channel and floating gate for program / erase tunneling.

Flash operation requires many clock cycles and command executions like the operation of internal state machines, data and command registers, high voltage generators, a.s.o.

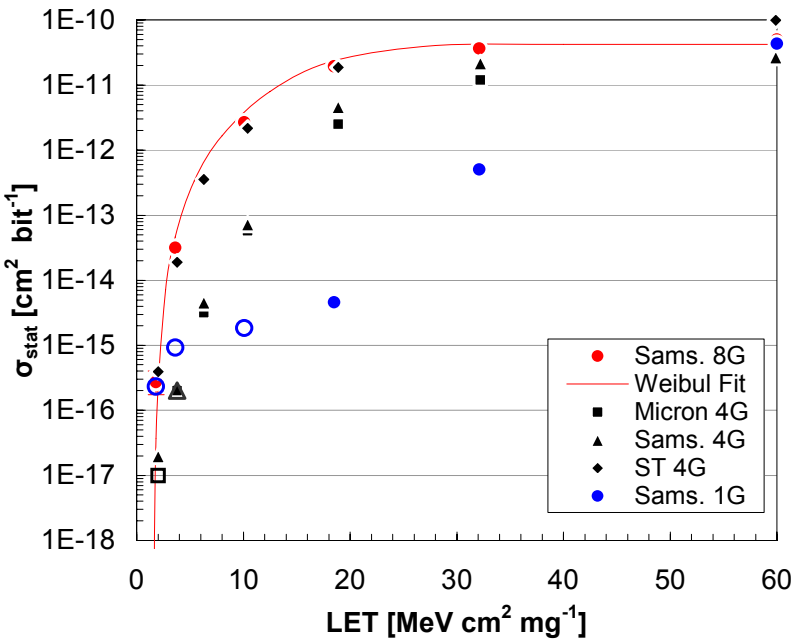
⇒ Numerous **potential** error types
besides the corruption of the content of storage cells.

⇒ Classification of **observed** errors needed.

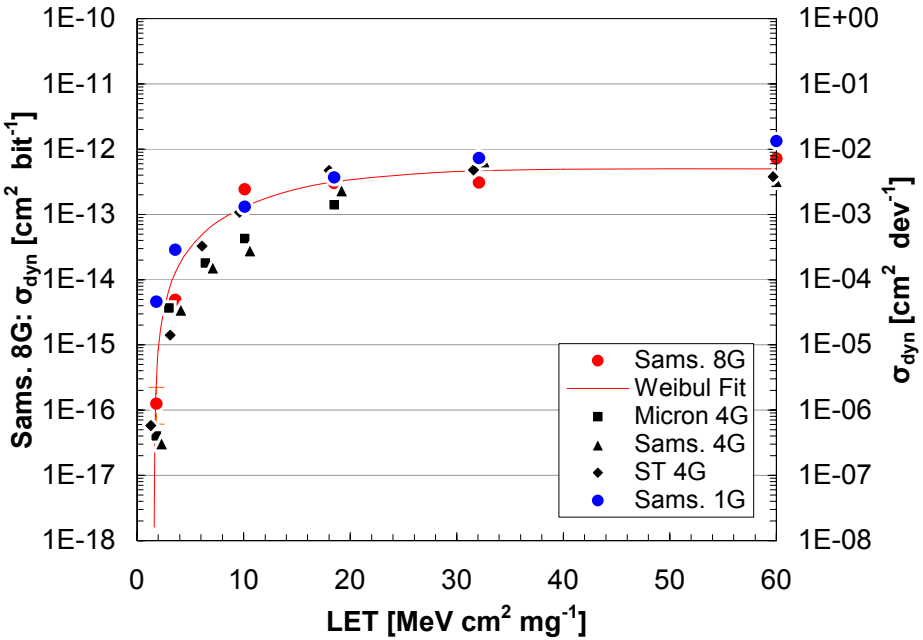
Error Classification Scheme



Heavy Ion Induced Single Errors (Class A)



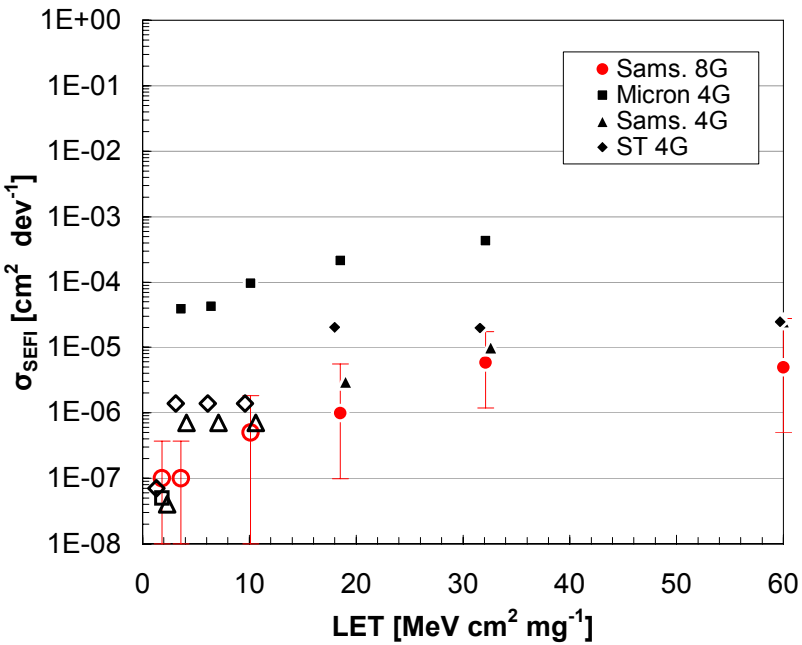
Static Errors, Storage Mode*



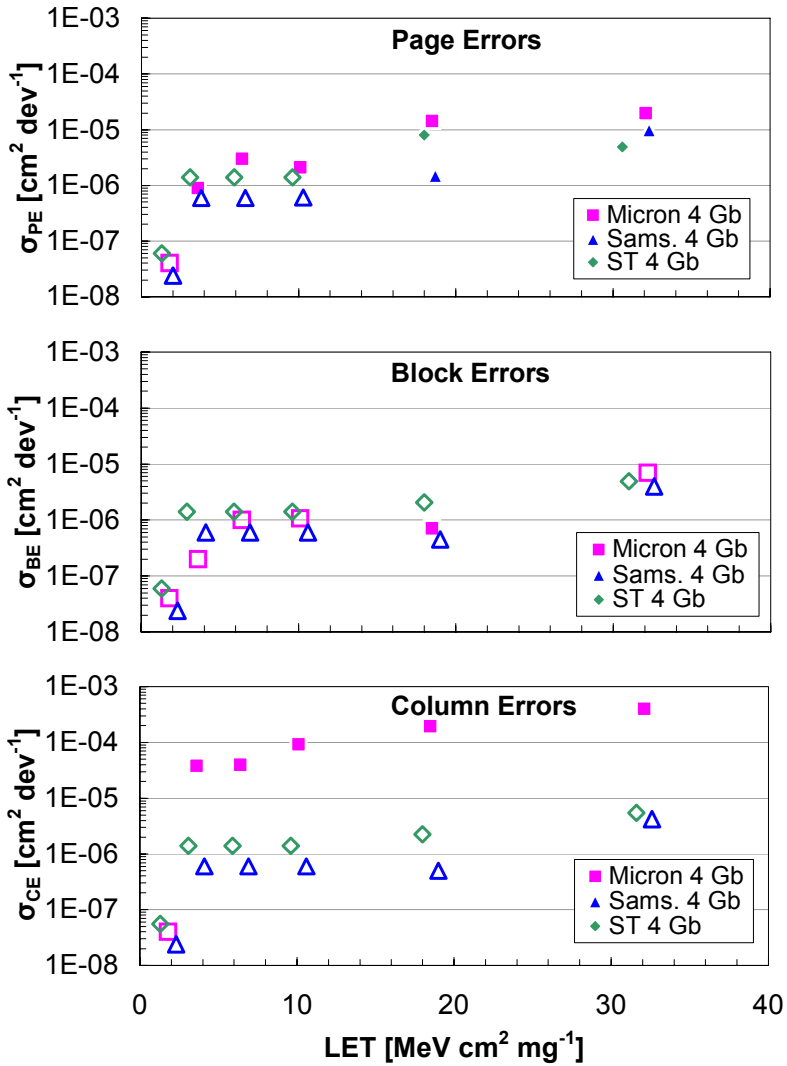
Dynamic Errors, Read Mode*

*: Open Symbols indicate "no errors up to this cross-section"

Heavy Ion Induced SEFIs (Class B+C)



Class B + C SEFIs, Read Mode*



*: Open Symbols indicate "no errors up to this cross-section"

Heavy Ion Induced Destructive Failures of the Samsung 8 Gbit NAND Flash

a) SELs have not been observed up to Xe (LET = 60 MeV cm^2 mg^{-1})

b) Other Destructive Failures (DF) have been observed only in test modes, which include erase and program operations.
Biased DUTs, during the irradiation non-accessed or only read-accessed , did not show any DFs.

c) Power cycling after each erase improves the DF cross section substantially. Using this countermeasure the threshold LET is situated between Fe (LET = 18) and Kr (LET = 32).

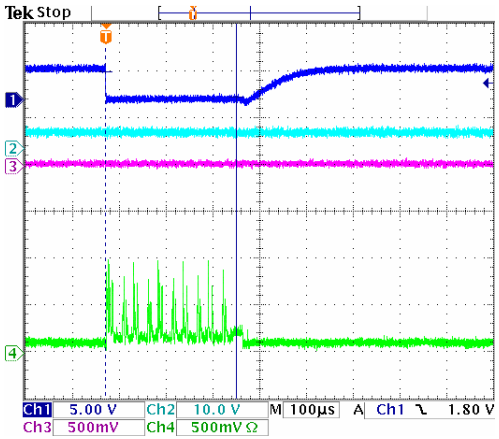
d) The program current grows in steps with the fluence,
until it reaches a characteristic final waveform, which soon is followed by a DF.

e) The waveform of the program current changes from page to page.

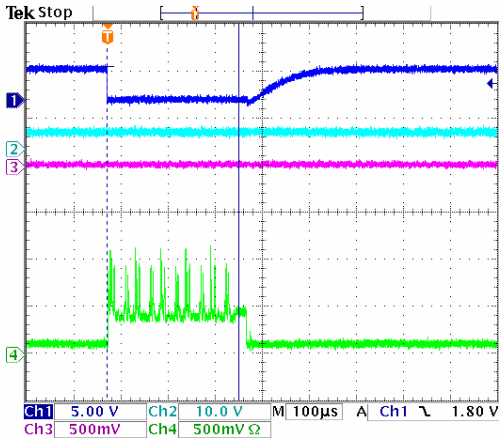
From d) and e) we conclude that the observed DFs were caused by accumulation of ion induced defects, which at least in part did anneal during the irradiation.

Faroukh Irom and others reported a thermal destruction of the high voltage generator, which they could avoid by shielding its area.
In contrast e) suggests that the over-current stress of the high voltage generator originates from an accumulation of leakage points within the cell array.

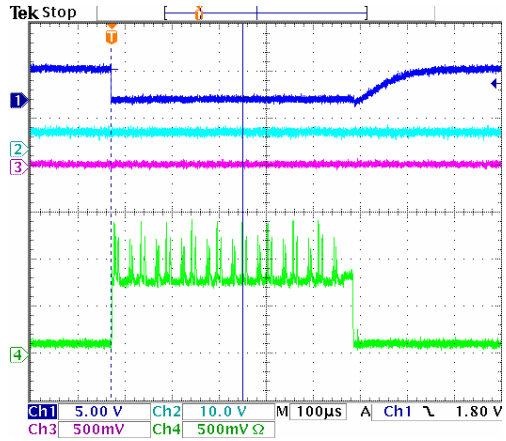
Development of the Program Current until DF Occurrence



Initial

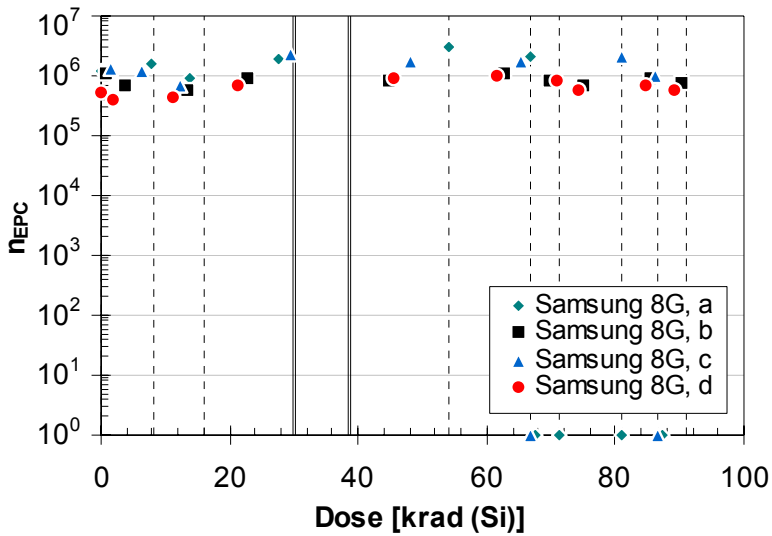


Increase with fluence



Final

Wear Out Limit not degraded by Co-60 TID

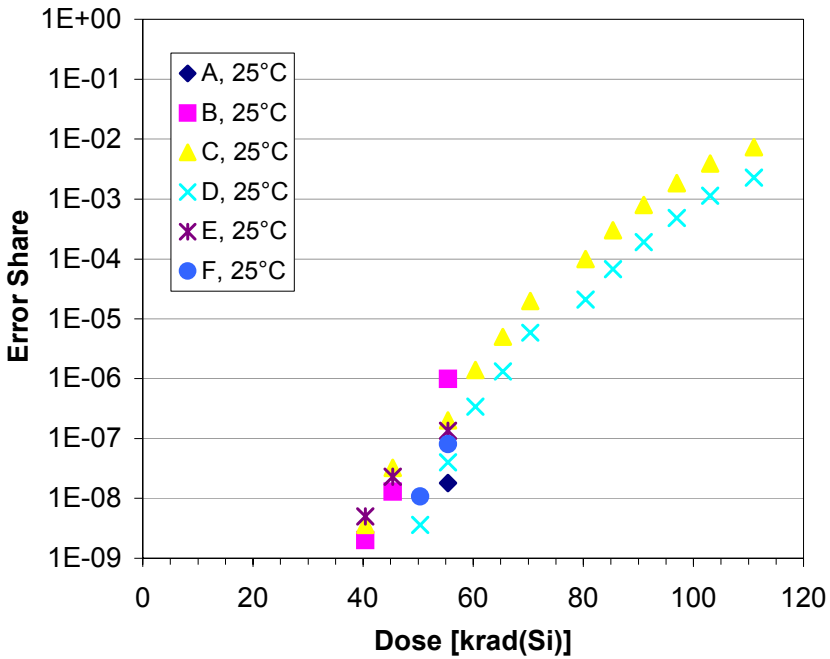


No degrading of the wear out limit with dose

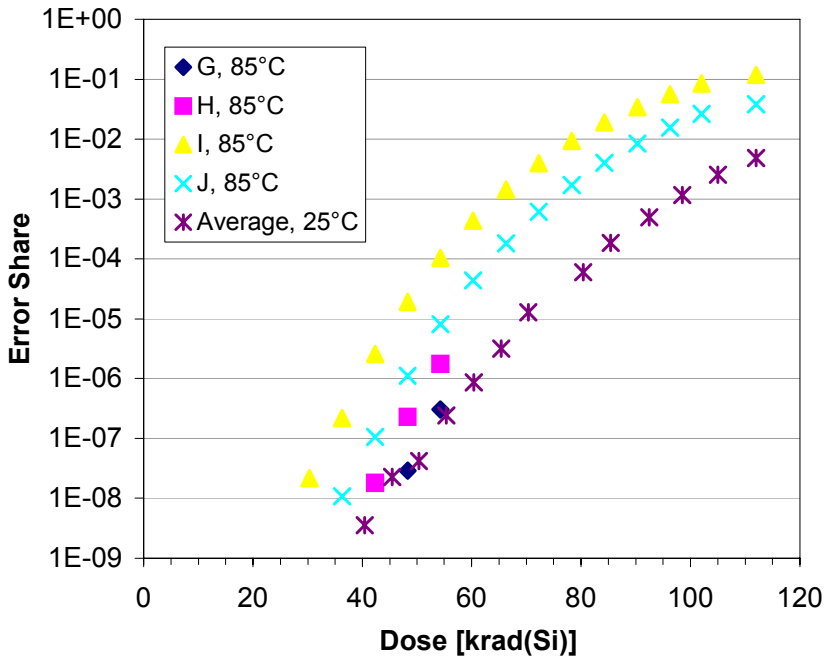
Number of Erase-Program-Cycles n_{EPC} until Wear Out,
Samsung 8 Gbit, 4 DUTs

TID induced Single Errors

DUTs not accessed during Co-60 γ-irradiation show the first Single Errors at about 40 krad at ambient temperature, and at about 30 krad for DUTs at 85°C.



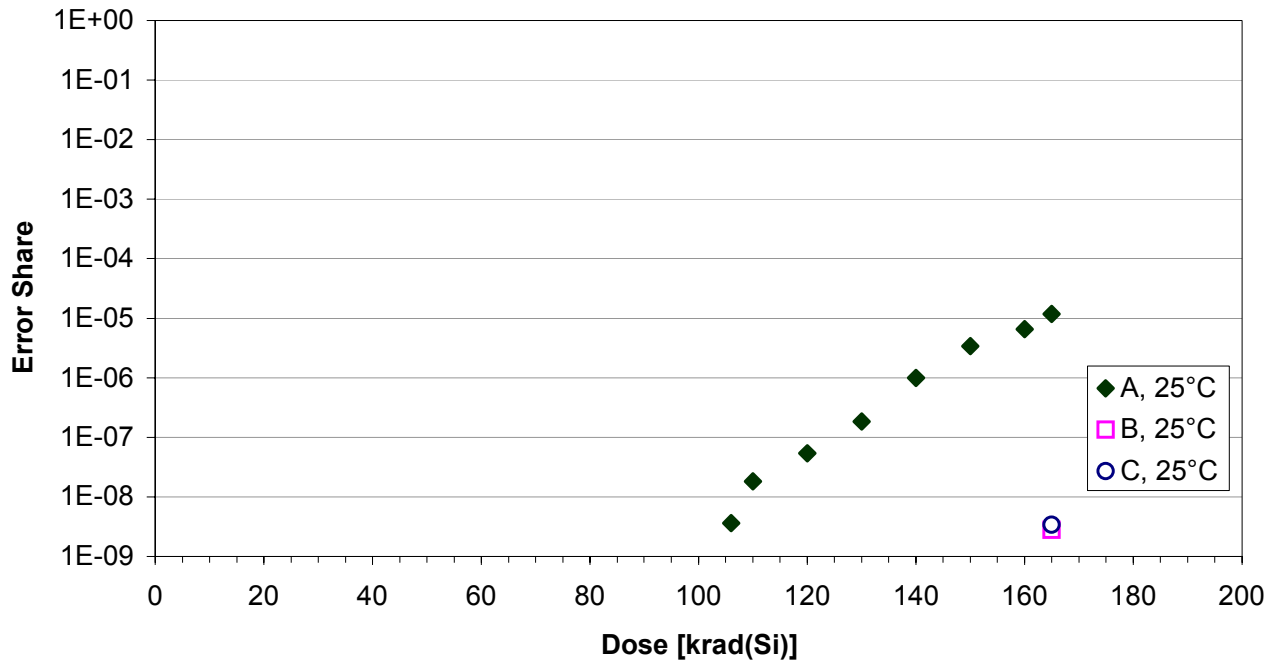
Biased Storage Mode, 135 rad min^{-1}, 25°C



Biased Storage Mode, 135 rad min^{-1}, 85°C

TID induced Single Errors

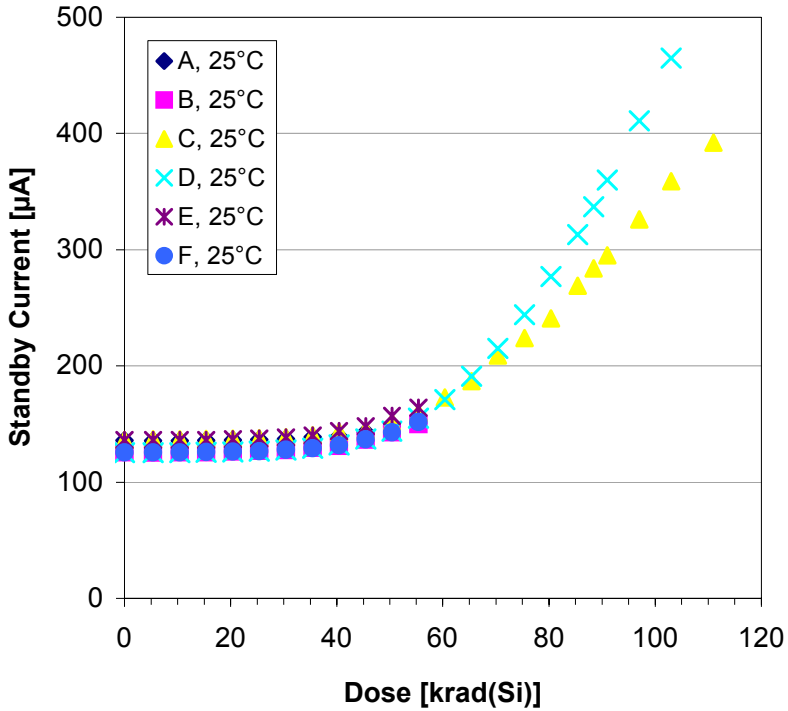
DUTs refreshed every 5 krad show the first Single Errors between 100 krad and more than 160 krad at ambient temperature.



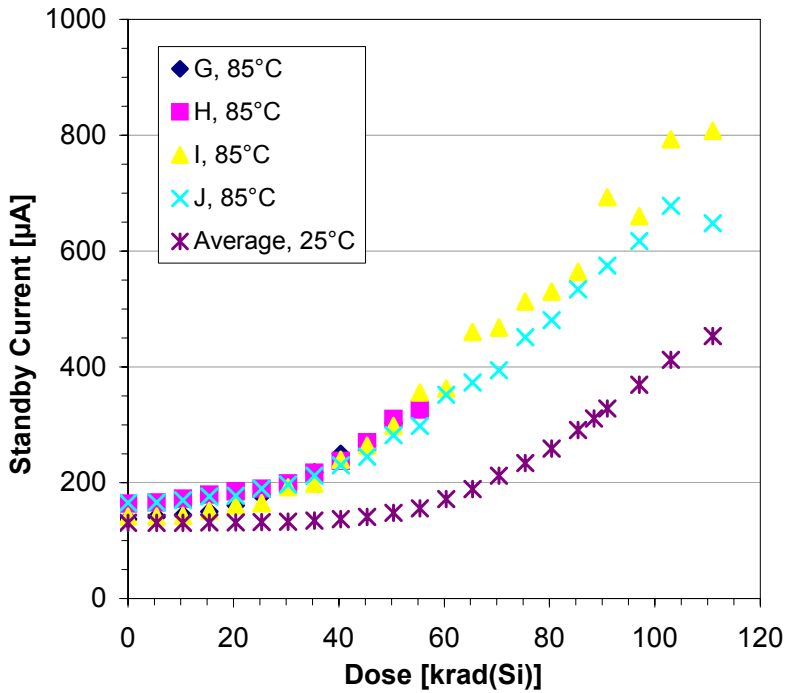
Biased Storage Mode, 5 krad Refresh *

*: Open Symbols indicate “no errors up to this dose”

TID induced increase of the Standby Current



Biased Storage Mode, 135 rad min^{-1}, 25°C



Biased Storage Mode, 135 rad min^{-1}, 85°C

Issues to be studied further

Heavy Ions, Protons, TID:

- **Survey of newcomers on the market (Micron 8 Gbit, …..).**
- **Temperature dependence of SEE and TID test data (cross section, standby current).**

Heavy Ions:

- **Destructive Failures**
  - **a) Cross Section curve of 8 Gbit NAND-Flash**
    Test data of more DUTs are needed.
  - **b) Upgrade of the test bed for automatic recording of read, program and erase current waveforms of selected pages / blocks, and performing of respective tests.**
  - **c) Test of potential countermeasures against Destructive Failures.**
  - **d) Flux dependence of cross sections**

- **Omni directional particle incidence in space,**
  High LET ion tests with tilting around two orthogonal axes.

TID:

- **Effect of Erase after 10 krad, 20 krad, 40 krad?**
- **Test at intermediate temperatures, e.g. 40°C, 60°C, 75°C ?**
- **Time consuming tests at lower dose rate, e.g. 1 rad min^{-1}, 0.1 rad min^{-1}.**

Acknowledgement

This work is in progress under ESTEC Contract No. 21711/08/NL/PA
to IDA TU Braunschweig and is supported by EADS Astrium.

We recognize gratefully the support given by the staff of UCL and RADEF, and in particular by Reno Harboe Sorensen and Bob Nickson of ESA, ESTEC and by Daniel Peyre and Christian Binois of EADS Astrium.