Heavy Ion SEE Test of an Advanced DDR2 SDRAM

L. Li, H. Schmidt, T. Fichna, D. Walter, K. Grürmann, H-W. Hoffmeister, S. Lamari, H. Michalik, and F. Gliem

***Abstract*—We report on a Heavy-Ion-SEE-Test of an 1-Gbit DDR2-SDRAM. DUT-preparation, design of the test equipment and first test results are described.**

***Index Terms*—DDR2, SDRAM, Heavy Ions, SEE, Die Thinning.**

I. Introduction

TODAYS space borne mass memories are based on volatile Synchronous Dynamic Random Access Memory (SDRAM) devices [6 - 8]. The steady speed growth of commercial processors enforced a steady increase of the SDRAM data rate. State of the art single die DDR2-SDRAMs range between a capacity of 1 Gbit at a data rate of 1 Gbyte/s or 2 Gbit at 650 Mbyte/s. A device internal Delay Locked Loop (DLL) is used to fine tune the phase between the edges of the external clock signal and the internal data strobes. Both, the rising and the falling edge of the clock are used for data transfer. An external clock rate of e.g. 250 MHz refers to a data rate of 500 Mbyte/s.

DDR2 devices offer a low stand-by power consumption, reduced by a factor of two compared to previous SDRAMs. Further progress in SDRAM device capacity is expected only for the DDR2 design line. Therefore, future SDRAM based mass memory designs might be dependent on DDR2 devices.

Space borne mass memories are designed for substantially lower data rates compared to work space memories for direct processor access. Operating the extended device arrays of a large mass memory with unnecessary high internal data rates would impose significant design complications and would waste power. Therefore, operation with a clock and data rate below the DLL window, i.e. with DLL OFF is an interesting option for DDR2 use in space borne mass memories.

NAND-Flash memory devices offer another alternative. They are designed for moderate data rates, a read rate of 25 Mbyte/s and a significantly slower write rate of 1 Mbyte/s, which by interleaving can be increased to a system write rate of 4 Mbyte/s times the bus width in bytes.

But, data rates above 1 Gbyte/s will remain to be the domain of DDR2 like SDRAMs. Therefore, radiation tests of state of the art devices of both memory technologies have to be performed and in consequence, dedicated test equipment has to be built for three types of radiation tests: (i) Heavy Ion Single Event Effect (SEE) tests, (ii) Proton SEE tests and (iii) Total Ionizing Dose (TID) tests using the simulation of protons and heavy ions by ^{60}Co γ-ray 1.17 MeV and 1.33 MeV photons.

Heavy ion tests simulate the bombardment of electronic devices with Galactic Cosmic Ray (GCR) ions. These charged particles originate outside of our solar system, most likely from supernova explosions. The energy of GCR particles is in the GeV and TeV range and even higher. In consequence GCR ions penetrate any feasable shielding. The omnidirectional staedy flux of GCR ions is a few cm-2 s-1.

A single GCR particle generates by ionization a track of mobile charges along its path through the die material. If a certain amount of those mobile charges is collected by a sensitive node, then a device malfunction will be triggered. These malfunctions are called Single Event Effects (SEE). So e.g. the state of a memory cell can be changed by a single particle hit.

The Linear Energy Transfer value (LET) (also called Stopping Power) is a metric for the energy loss of the penetrating particle. The energy loss per distance unit dE/dx is proportional to the charge density dQ/dx and therefore, proportional to the LET value of the penetrating particle.

$$\mathrm{LET} = \frac{\mathrm{dE}}{\rho \cdot \mathrm{dx}} \qquad \left[\frac{\mathrm{MeV}}{\mathrm{mg/cm^3} \cdot \mathrm{cm}} = \mathrm{MEV} \cdot \mathrm{cm^2/mg}\right]$$

$$\frac{\mathrm{dQ}}{\mathrm{dx}} = \mathrm{k} \cdot \frac{\mathrm{dE}}{\mathrm{dx}} = \mathrm{k} \cdot \rho \cdot \mathrm{LET} \qquad \left[\mathrm{fCb/\mu m}\right]$$

The LET value of an ion depends on both, its energy and its mass (Fig. 1). Usually the ion energy is counted in MeV per nucleon.

The LET value increases with the ion mass and decreases with energy behind the Bragg Peak (Fig. 1).

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The mass spectrum of GCR ions drops very steeply after the Fe peak. Higher mass ions are so rare that they can be neglected for practical design purposes.The Bragg peak for Fe is roughly at 30 MeV cm^2 / mg. In consequence the LET range of the test ions can be restricted to LET values up to 60 MeV cm^2 / mg, i.e. up to Xe.

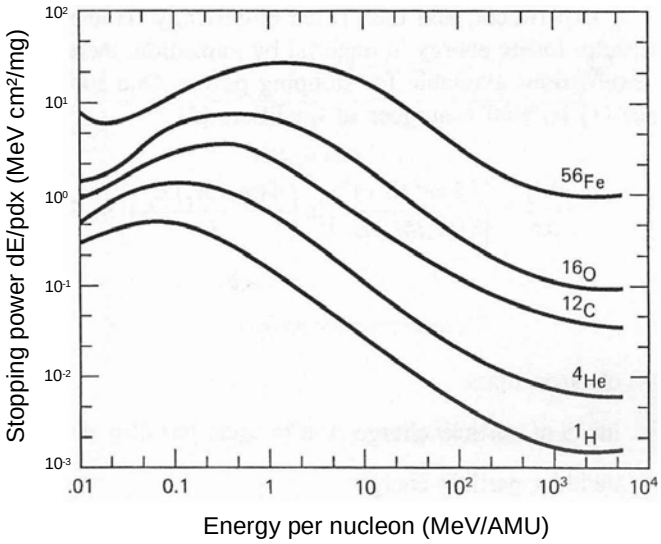

Fig. 1. LET as function of ion energy and ion mass

In our previous paper [10] the Heavy Ion test of NAND-Flash devices was treated. Here, we report on a recent Heavy Ion SEE test of an 1 Gbit DDR2 device with DLL OFF, and in particular on the intricate preparation of the Devices Under Test (DUT) and on the dedicated test equipment.

II. Organization of the Memory Array

The 1G storage cells are organized into 8 banks of 16k rows each, of 256 columns each, of 4 bytes each. Accordingly, the 27-bit address is subdivided into 3 bank selection bits, 14 row selection bits, 8 column selection bits and 2 byte selection bits. Internally 4 bytes are stored at once. An internal state machine executes the byte sequencing, the refresh, the externally initialized device status and several other control actions.

III. Test Facility

The tests were performed at the Heavy Ion Facility (HIF) of the Cyclotron Research Center (CRC) of the Universite Catholique de Louvain (UCL), Belgium. To penetrate the active regions of the die via backside irradiation the High Penetration Cocktail with M/Q ≈ 3.3 was used (Table I(a)).

TABLE I(A)
HIGH PENETRATION COCKTAIL AT HIF/UCL

Ion	Energy [MeV]	Range [μm_{Si}]	$LET_{init.}$ @0µm Si [MeV mg^{-1} cm^2]	$LET_{eff.}$ @70µm Si [MeV mg^{-1} cm^2]
$^{13}C^{4+}$	131	266	1.2	approx. 1.5
$^{22}Ne^{7+}$	235	199	3.3	3.9
$^{40}Ar^{12+}$	372	119	10.1	14.3
$^{58}Ni^{18+}$	567	98	20.6	31.6
$^{83}Kr^{25+}$	756	92	32.4	40.9

TABLE I(B)
HIGH PENETRATION COCKTAIL AT RADEF/JYVL

Ion	Energy [MeV]	Range [μm_{Si}]	$LET_{init.}$ @0µm Si [MeV mg^{-1} cm^2]	$LET_{eff.}$ @70µm Si [MeV mg^{-1} cm^2]
$^{15}N^{4+}$	139	202	1.8	approx. 2.0
$^{20}Ne^{6+}$	186	146	3.3	4.8
$^{30}Si^{8+}$	278	130	6.4	8.2
$^{40}Ar^{12+}$	372	119	10.1	14.3
$^{56}Fe^{15+}$	523	97	18.5	27.3
$^{82}Kr^{22+}$	768	94	32.1	40.5
$^{131}Xe^{35+}$	1217	89	60.0	61.5

IV. DUT Preparation

The DDR2 memory dies are housed in plastic encapsulated ball grid packages (60ball FBGA) to accommodate the high data byte rate of 250 MHz/s. Fig. 2 shows the conceptual package diagram.

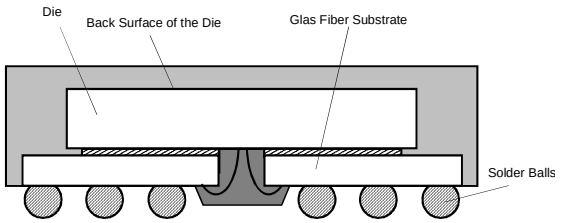

Fig. 2. Conceptual Diagram of the FBGA Package.

The die is situated upside down. Bonding wires connect pads along the longitudinal die axis with their counterparts on a glass fiber substrate, which distributes the signals to the solder ball grid underneath the base plane of the package. The uncomfortable consequence is that removal of the cover plastic gives access only to the back surface of the die and not to its sensitive top surface. The penetration of the ion beams available at the Heavy Ion Facility (HIF) at Universite Catholique de Louvain (UCL), Belgium [7, Table I(a)] and at the Radiation Effects Facility (RADEF) at University of Jyväskylä (JYFL), Finland [7, Table I(B)], e.g. an ion range of 90 µm at LET ≈ 30 MeV cm^2 mg^{-1}, is substantially below the die thickness of about 200 µm. In consequence ions irradiated from the backside can not reach the sensitive structures below the top surface of the die. To make this possible, the die has to be opened and thinned.

The cover plastic has been removed by drop etching with fuming nitric acid. The device is fixed to a mounting plate and is covered with Teflon tape. A window is cut into the tape. Then the device is heated up to about 70°C. An acid drop is placed into the window and then the device is rinsed with wa-

ter and acetone. This step of etching and rinsing is repeated many times until the die surface is free of plastic.

The thinning of the die has to be enforced such that Xe ions will penetrate the die until the active die zones below the top surface of the die, i.e. to a die thickness of less than 80 µm. On the other hand thinning makes the die more fragile, and sufficient distance from the active die zones has to be kept. In particular the latter aspect is important with respect to the sensitivity of the device against heavy ion induced Latch Ups. A Latch Up is triggered if a sufficient amount of parasitic charge is collected at a sensitive node. The collection process is fed by funnelling of ionization charges, which are generated along the ion track in the bulk silicon below the active zone. Therefore, to much enforced thinning could fake a Latch Up immunity of the device.

Both, successful and unsuccessful thinning efforts have been reported [2], [5]. After some unsuccessful attempts we exercised thinning from an initial die thickness of 205 µm down to 70 µm without any impairment of the functionality. The opened device was fixed to a metallic support structure by few small adhesive pads (Fig. 3).

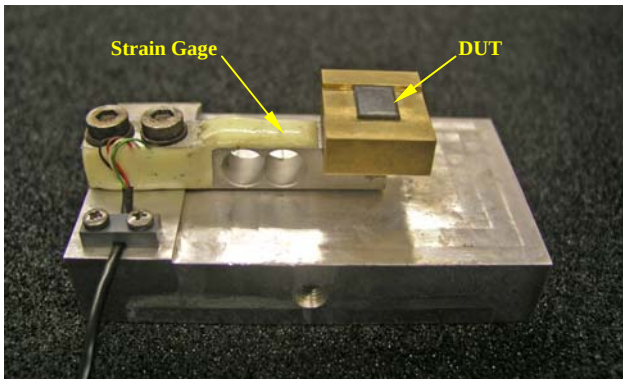

Fig. 3. Mechanical DUT Support Structure

The force applied by the grinding tools was monitored by a strain gage on top of the support lever. Grinding wheels were used such as applied for the separation of wafers: (i) diameter 52 mm, (ii) thickness 500 µm and (iii) a tip profile of 120° in order to reduce the contact volume and thereby, the grinding forces. The synthetic diamond grains with a medium grain diameter of 5 µm were supported by a bronze bond. Using the following grinding parameters the die could be machined from an initial thickness of 205 µm to a final thickness of 70 µm, (i) infeed speed 100 mm/min, (ii) cutting speed 60 m/s, (iii) grinding width 20 µm. The grinding depth per path was varied in 6 steps: 25 µm for the first four steps, and for the final two passes 20 µm and 15µm, respectively. In the clamping the die showed a curvature of 5 µm in lateral extension and of 10 µm in longitudinal extension. Therefore, the path of the grinding wheel had to be adapted to this curvature. By grinding in lateral direction the larger one of the two shape deviations could be reduced definitely. For the chosen setting parameters the grinding time took 8 hours per device.

V. Memory Test Equipment

The RTMC-4 Testbed for Memory Components is structured into three subunits (Fig. 4): (i) DUT Test Adapter (DTA), (ii) Fast Test Unit (FTU), distance to DTA ≤ 5m, extendable by USB hubs and (iii) Remote Control Unit (RTU), distance to FTU ≤ 100 m.

Fig. 5 displays the DTA board. It is structured into two sections. In the lower section up to eight DUTs can be placed. In this case we see four thinned Micron 1-Gbit DDR2 devices. The upper section will be shielded during γ-photons or protons exposure. This section contains all the circuitry, which needs to be situated close to the DUTs, mainly for speed reasons. The shown RCU board supports two DUT clock rates: 25 MHz for operation with DLL OFF and 200 MHz for operation with DLL ON.

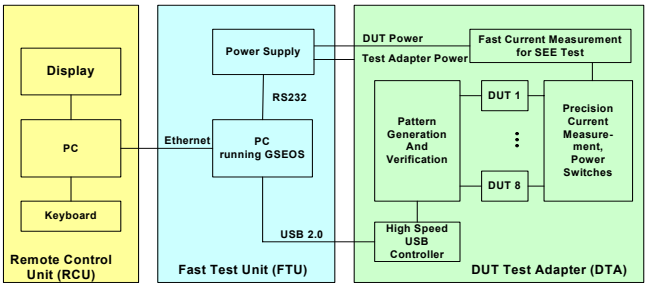

Fig. 4. Overall Structure of the RTMC-4 Memory Testbed.

The core functions of the FTU are implemented in a Xilinx Virtex-4 FPGA. In particular the FPGA contains memory controllers, pattern generation and verification and Latch-Up control. The maximum static address width is 28 bit, and the maximum dynamic address width is 24 bit row + 24 bit column. The maximum data width is 16 bit.

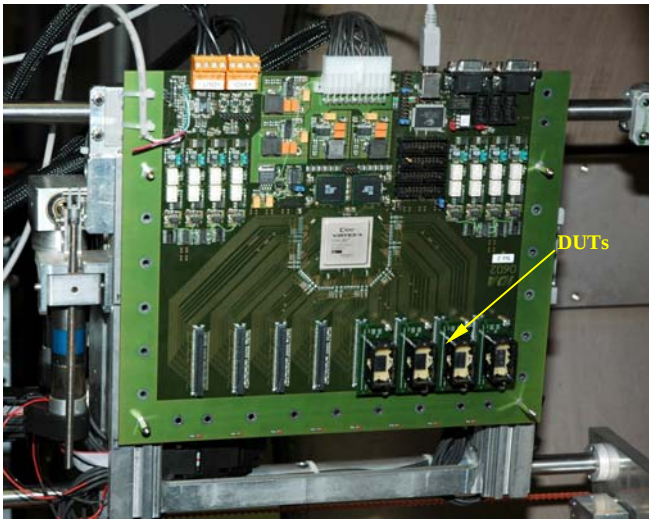

Fig. 5. DTA populated with four DUTs.

Several address patterns are selectable such as Read Background, Write Background and Marching, and also several

data pattern such as Constant (128 bit word), Counting (Up and Down) and Pseudo-Random (128 bit seed). Each data pattern is selectable to be inverted.

In real time for each error an error vector (128 bit) is produced and is stored in an error buffer FIFO with a capacity of 128 k error vectors, for later transfer to the FTU hard disk.

During SEE tests the DUT current is continuously monitored by a high speed low (4 mA) resolution ADC, and during TID tests by a low speed high resolution (switchable between 10 pA and 100 µA) ADC. The DUT supply voltage is adaptable between 1.5 and 5.0 V, and the I/O voltage between 1.5 and 3.3 V.

Fig. 6 shows the RCU. Its display provides real time monitoring of all test parameter settings, error counts, error statistics as error distribution over the bit planes, percentage of zero to one and one to zero falsifications, and in particular a map of the error distribution over the address space in real time (Fig. 7.)

Fig. 6. RCU situated in the Control Room.

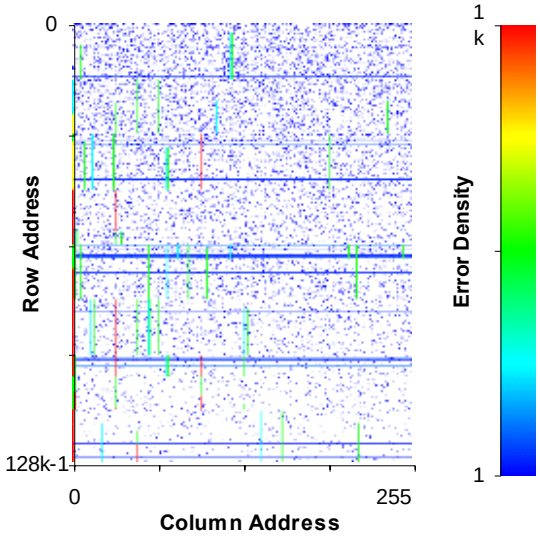

Fig. 7. Error Map of a selected Bit Plane.

The 256 image columns represent the 256 device columns per bank. The 512 image rows represent the 8 x 16k device rows, i.e. all errors in. 8 x 32 rows are displayed by one image row. Color coding gives an impression of the error density. The example error map shows (i) distributed single errors, (ii) horizontal error sequences and (iii) vertical error sequences.

Single errors can be traced back to particle hits of array cells, and extended error sequences to Single Event Functional Interrupts (SEFI), which are caused by particle hits of the device internal control circuitry.

VI. Test Goal

The primary goal of our June 2008 test campaign at UCL was to verify the proper function of the new testbed. Further we started the Heavy Ion SEE characterization of the advanced Micron 1-Gbit DDR2 SDRAM MT47H128MBMQ, with focus on its DLL OFF operation at the application driven reduced clock rate of 25 MHz.

VII. Test Results

The DUTs, all running with 7.8 µs Auto-Refresh row to row at ambient temperature with DLL OFF at 25 MHz clock rate, were exercised in three test modes:

1. Storage Mode M3:
   Write checkerboard before irradiation, no access during irradiation, read after irradiation.
2. Write Mode M4a:
   A checkerboard pattern is written before irradiation. During irradiation an inverted checkerboard is written, which takes about 20s. Thereafter the beam is switched off and the stored data are read and verified. No DUT S/W Conditioning [2] during irradiation.
3. Write Mode M4b:
   As before, but DUT S/W Conditioning after eight rows, each.

S/W Conditioning refreshes the device status with the intention to reduce SEFI induced data corruption.

Fig. 8 shows the Single Bit Error Cross Section for operation in Storage Mode M3 and in both Write Modes M4a/b. SEFI related bit errors are not taken into account. In consequence both modes M4a and M4b deliver the same cross section. Also, the M3 cross section is alike the M4a/b cross section. This indicates that nearly all bit errors originate from the cell array. For comparison the single bit cross section of the 1 Gbit Micron device in Read Mode, DLL ON, 200 MHz, [9] is added. For both, Single Bit Errors and SEFIs we see a much larger cross section at loe LETs, which possibly originates from hits of the DLL circuitry.

Fig 9 gives a comparison with the single bit error cross section of other SDRAMs. Apparent is the rather good congruence with the Samsung 512-Mbit DDR2 SDRAM.

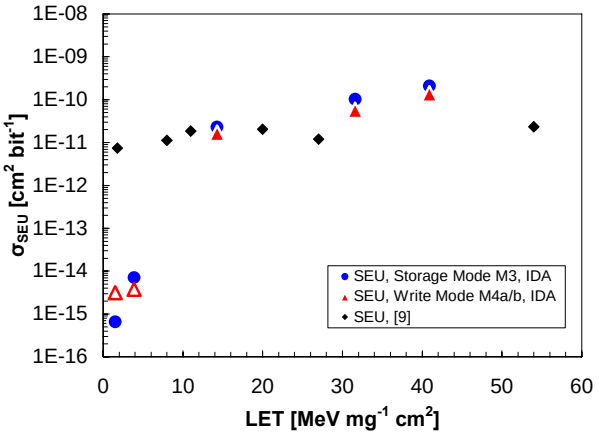

Fig. 8. Single Bit Error Cross Section, Micron 1-Gbit DDR2 SDRAM, DLL OFF, 25 MHz, [IDA]; DLL ON, 200 MHz, [9].

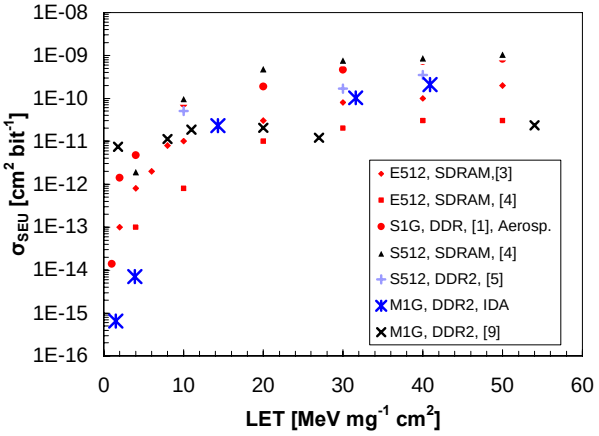

Fig. 9. Single Bit Error Cross Section, Micron 1-Gbit DDR2 SDRAM, DLL OFF, 25 Mhz. Comparison with other SDRAMs.

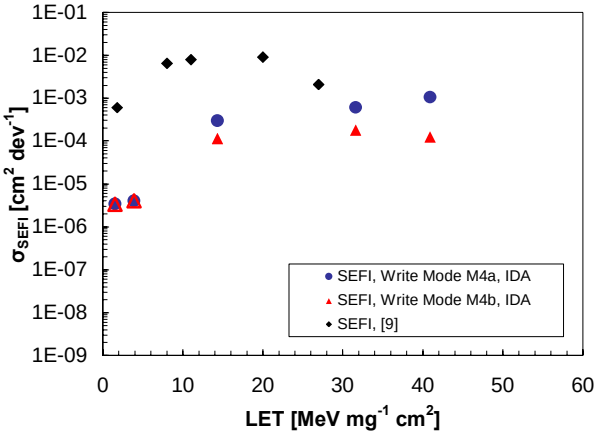

Fig. 10. SEFI Cross Section in Write Mode, Micron 1-Gbit DDR2 SDRAM, DLL OFF, 25 MHz, IDA; DLL ON, 200 MHz [9].

Fig. 10 shows the SEFI cross section in both Write Modes, M4a without S/W Conditioning and M4b with S/W Conditioning. For comparison the SEFI cross section in Read Mode without S/W Conditioning [9] is added, also. The positive effect of S/W conditioning is apparent. Fig. 11 presents a comparison with SEFI cross sections of similar devices.

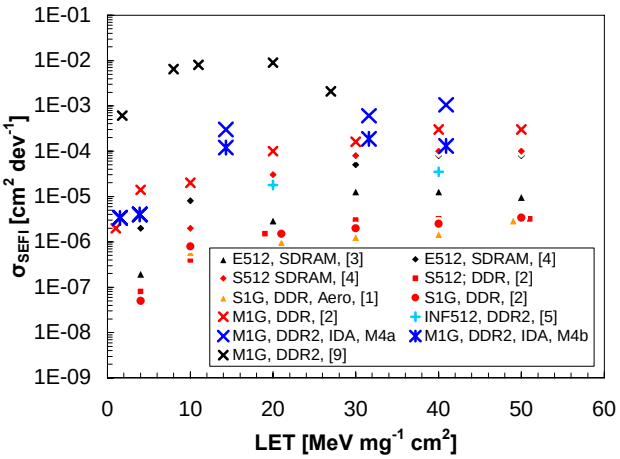

Fig. 11. SEFI Cross Section in Diverse Test Modes, Comparison with other SDRAMs.

VIII. Summary

A method of die thinning by grinding from initially 200 µm to 70 µm and the main features of a new memory testbed are described. Results of a Heavy Ion SEE test of a 1-Gbit Micron DDR2 SDRAM with DLL OFF are reported. The gained cross sections are alike those of previous SDRAM generations.

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